Contents

Chapter 4: 5300ET Electronic Timer Module

Chapter 5: 5300 Master Oscillator Module

Chapter 6: 5300MB Modem Board

Chapter 1

Frame Overview

1.1 Introduction

The CSD-5300 Clock System Driver is designed to be a central source of time for broadcast or computer facilities. It operates as a high stability stand alone clock. If required, it will automatically update its time from a central standard. The CSD-5300 unit provides the following outputs:

3. SMPTE/EBU Serial Time Code, 600 Ω bal.
4. SMPTE/EBU Serial Time Code, Low Z bal.
5. Serial BCD Time
6. 1 Hz
7. 60/50 Hz
8. 2-phase, 12/24 VDC Impulse Drive
9. Parallel BCD Time
10. 1 MHz / 100 kHz (jumper selectable)
11. 5 MHz Sine Wave, 75 Ω, 2 Vp-p
12. Time Markers, 600 Ω bal.
13. Time Markers Present
14. Time and Date, ASCII 300 baud, Bell 103 Modem (on demand)
15. Time and Date, ASCII RS232 300 baud (on demand)

1.2 Specifications

Inputs

External Reference

Frequency	5 or 10 MHz
Level	2 Vp-p ±3 dB
Impedance	75 Ohms, loop-through

External Strobe

Input	contact closure or logic level falling edge
Logic levels	TTL compatible

Outputs

SMPTE /EBU Time Code

Format		SMPTE/EBU (nondrop frame)
Output 1	Level	+10 dBm nominal unloaded, -3 dB into 180 Ohms
	Impedance	Low-Z, balanced
Output 2	Level	+4 dBm nominal
	Impedance	600 Ohms, balanced

RS232 Interface

Interface type	data set
Baud rate	300
Parity	none
Data format	8 bits, 1 stop bit

BCD Parallel Time

Data format	BCD parallel frame count, seconds, minutes and hours
Level	5 volt logic levels
Drive capability	4000 Series, CMOS outputs.

BCD Serial Time

Data format	BCD serial frame count, seconds, minutes and hour with related clock and latch pulses
Clock format	data valid on falling edge of clocks

BCD Serial Time (Cont.)

Latch format	active low pulse at end of frame
Level	5 volt logic levels
Drive capability	HC CMOS outputs (LSTTL compatible)

Marker Beeps

Frequency	1200 Hz (1000Hz for EBU)
Duration	0.3 second
Timing	1 pulse on the hour, double pulse on the half hour with 0.3 sec. spacing. Separate enable for each signal.
Level	8 dBm nominal
Impedance	600 Ohms balanced

Tone Present

Output	High during tone output
Level	+5 V logic levels
Drive capability	HC CMOS output (LSTTL compatible)

Reference Outputs

Output 1 Frequency	5 MHz
Level	2 Vp-p
Impedance	75 Ohms
Output 2 Frequency	100 kHz / 1 MHz square wave (jumper selectable)
Level	5 volt logic levels
Drive capability	HCCMOS output (LSTTL compatible)

1Hz, 60Hz/50Hz

Frequencies	1Hz, 60Hz/50Hz square waves
Level	5 volt logic levels
Drive capability	HC CMOS output (LSTTL compatible)

Time Valid

Output	active high
Level	5 V logic levels
Drive capability	HC CMOS output (LSTTL compatible)

Telephone Interface

Format	Bell 103 compatible, originate and answer modes
Modem	autoanswer, autodial with speaker and volume control
Dialing capability	up to 25 digits, DTMF, pulse or combination with programmable interdigit delay.
Receive sensitivity	-50 dBm
Transmit level	-10 dBm
Connector	modular jack, compatible with RJ11, RJ12 and RJ13 type jacks

Impulse Drive

System	2-phase, +12/24 VDC
Maximum load	25 impulse clocks
Drive protection	current limiting
Clock correction after power failure or shorted outputs	automatic

Performance

Oscillator aging	<5 parts in 108 per month
Oscillator stability with 10% line voltage variation	<1 part in 108
Oscillator stability with temperature change from 0° to 50°C	<1 part in 108
Oven warm up time	<20 minutes
Time acquisition accuracy	
Over telephone line	<1 ms of source *
Using external strobe	<20 µs of strobe
Compensation for telephone line loop delay	automatic
Detection of asymmetric loop	automatic with user definable parameters
External standby battery capability	unit fully operational
Internal standby battery capability	timekeeping only for over 8 hours (no outputs enabled).

**** Under normal telephone line operating conditions. Operation in extraordinary conditions cannot be guaranteed.***

Temperature Range

Operating	0-50°C
Performance	5-40°C

Electrical

Line Voltage	95/135 VAC
Frequency	60 Hz/50Hz
Power Consumption	20 VA
External standby battery Voltage	20-26 V
Power Consumption	15 W

Mechanical

Height	44 mm (1.75 inches)
Width	483 mm (19 inches)
Depth from mounting surface	290 mm (11.5 inches)
Overall depth	320 mm (12.5 inches)
Weight	5.7 kg (12.5 lbs.)

Specifications and designs are subject to change without notice.

1.3 Installation

The CSD-5300 Clock System Driver is carefully inspected, tested and calibrated before shipment to ensure stable and trouble-free service. Please check the unit for any visible damage which may have been caused during transit. Ensure that the modules have remained properly seated in the mounting frame.

1.3.1 Mounting Requirements

The CSD-5300 unit requires 44 mm (1.75 inches) of standard 483 mm (19 inches) rack space. The minimum depth required behind the mounting surface is 290 mm (11.5 inches).

1.3.2 Cooling Requirements

The Clock System Driver is designed to meet specifications in an ambient temperature range of 5°C to 40°C. No special provisions for cooling are necessary, but care should be taken to prevent excessive heat rise in closed, unventilated equipment racks.

1.3.3 Power Supply

The power consumption of the CSD-5300 unit is 20 VA based on the normal module complement at nominally 95/135 VAC, 60 Hz/50 Hz. The driver is equipped with a detachable power cord and a resettable circuit breaker.

1.3.4 Internal Battery Supply

The CSD-5300 unit is equipped with an internal battery pack. In case of a power failure, only the time keeping circuitry is kept operational and all outputs are disabled.

The battery pack contains three 9 Volt batteries. If primary batteries are used, type MN1604 alkaline batteries or equivalent, are recommended. With this type of battery, the circuitry will operate for over 8 hours.

If secondary batteries are to be used, resistors can be added to the battery pack to allow charging.

NOTE: To prevent discharging of the internal battery supply, the battery pack is removed for shipment.

1.3.5 External Battery Supply

Provision is made to allow the connection of an external, user supplied, 24 Volt battery if operation of the entire unit is required during AC power failures. The connecting terminal block for the external battery is located on the rear panel.

1.3.6 5300ET Electronic Timer Configuration

The DIP switch on the front of the 5300ET module is used to configure many of the operational parameters of the CSD-5300 unit. All switches enable their corresponding function when in the up position. The DIP switch is connected as follows:

Switch	
1	Input HMS offset / AUX offset
2	Keyboard beep enable
3	Telephone system mode access enable
4	Telephone answer enable
5	Half hour tone enable
6	Hour tone enable
7	Impulse clock driver enable
8	Auto Change/Normal Mode Selection

For further details on the functions, please refer to the operation section of this manual.

1.3.7 Rear Panel Connections

Telephone Line

The telephone line connector is a standard 6-position, 4-wire modular jack, compatible with either wall or floor RJ11, RJ12 and RJ13 type jacks.

The CSD-5300 unit is prepared for connection to RJ11 type telephone jacks. If connection to RJ12 or RJ13 type jacks is desired, a jumper must be added on the 5300MB Modem Board module.

The jumper is positioned between relay K2 and transistor Q3 and adjacent to the edge connector pins of the 5300MB module.

IMPORTANT:

1. **Never install telephone wiring during a lightning storm.**
2. **Never install telephone jacks in wet locations unless the jack is specifically designed for wet locations.**
3. **Never touch uninsulated telephone wires or terminals unless telephone line has been disconnected at the network interface.**
4. **Use caution when installing or modifying telephone lines.**

Impulse Drive Output (3-position barrier strip)

Up to 25 impulse clocks may be connected to the impulse drive connector.

Time Code Output

The SMPTE/EBU Time Code output is available from either of two 3-position terminal blocks. The upper of the two connectors is a low impedance balanced output, capable of +10 dBm unloaded, dropping 3 dB into 180 Ohms. The lower connector is a 600 Ohm balanced output at +4 dBm nominal.

Since clocks such as the LEITCH DAC-5000 Series Digital Analog Clocks bridge high impedance inputs, a large number of clocks may be connected in parallel to this output. However, for purposes of fault isolation, it is recommended that some form of distribution, such as that provided by the LEITCH ADA-800 Series Audio Distribution Amplifiers, be used when connecting more than 20 clocks to the system.

Auxiliary Output

The CSD-5300 unit uses a female 37-pin D connector on the rear panel for auxiliary outputs and external strobe input. The connector is wired as follows:

Pin		Pin	
1	Ground	21	Tone present
2	Time valid (active high)	22	Impulse clocks stopped
3	1 Hz	23	Serial time data
4	60 Hz/50 Hz	24	Frame Bit 0
5	Serial time clock	25	Frame Bit 2
6	Frame Bit 1	26	Frame Bit 4
7	Frame Bit 3	27	Seconds Bit 0
8	Frame Bit 5	28	Seconds Bit 2
9	Seconds Bit 1	29	Seconds Bit 4
10	Seconds Bit 3	30	Seconds Bit 6
11	Seconds Bit 5	31	Minutes Bit 1
12	Minutes Bit 0	32	Minutes Bit 3
13	Minutes Bit 2	33	Minutes Bit 5
14	Minutes Bit 4	34	Hours Bit 0
15	Minutes Bit 6	35	Hours Bit 2
16	Hours Bit 1	36	Hours Bit 4
17	Hours Bit 3	37	Serial Time Latch
18	Hours Bit 5		
19	100 kHz/1MHz		
20	External Strobe input (active low)		

All outputs from the auxiliary output connector are 5 Volt logic level signals.

The signals on pins 6 to 18 and 24 to 36 give the time in parallel BCD format. The output consists of frame count, seconds, minutes and hours. This output changes 30 times a second to reflect the new frame count. The time information output refers to the present frame, and is updated approximately 100ms before the start of each new frame. As an example, 100µs before noon the output will change from 11 59 59 29 to 12 00 00 00.

Three output signals are used to give the time in serial format. The Serial Time Data output on pin 23 contains the time information which is sent out 30 times a second. The data is sent in the same order as in the time code output, i.e. frame count, seconds, minutes and hours, with the LSB sent first. As in the time code output, the time data refers to the upcoming frame. The Serial Time Clock output on pin 5 goes high at the start of each data bit, and falls 208 µs

later. Data should be taken as valid on the falling edge of clock. The Serial Time Latch signal, on pin 37, pulses low approximately 100 ms before the end of each frame. This signal can be used by external circuitry to latch in the serial time data.

As an example, two frames before noon, the serial data output will be 11 59 59 29. During the frame immediately before noon, the serial data output will be 12 00 00 00.

The 1 Hz and 60 Hz/50 Hz outputs on pins 3 and 4 respectively are square waves. These signals are synchronous with the time output of the unit. At the top of each second, both outputs fall. Therefore, these outputs can be used to latch the correct time edge.

The 100 kHz/1 MHz output, on pin 19, is derived from the time base of the unit, but is independent of the time output. The output frequency on this pin is selected by the 100 kHz/1 MHz jumper on the 5300MO module.

The Time Valid output is high when the unit has valid time information. The Impulse Clocks Stopped output is high when the unit has stopped the impulse drive output. The Tone Present output goes high for the duration of any hour or half-hour marker tone output.

When a new time is being input, a 5 Volt logic-level falling edge input or a contact closure on the External Strobe line will synchronize the unit to the external time source. Only the first edge is taken for each separate time input operation. In other words, the unit will not continually accept synchronizing information from a pulse train. Refer to the Operation section of this manual for further information on the use of the External Strobe input.

To lessen the radiation of radio frequency energy and ensure compliance with Part 15 of the FCC rules, it is recommended that a shielded cable such as Belden 9519 be used for connections to the auxiliary output connector.

RS232 Connector

The RS232 interface uses a 25-pin female D connector on the rear panel of the CSD-5300 unit. Two communication ports are provided via this connector. One is for the standard terminal interface while the second accommodates the optional 5300RI Reference Interface module. Both ports may be connected at the same time, but only one will operate at a time. The 5300RI has priority.

The connector is wired as follows:

Pin	
1	Protective Ground
2	Serial Data In
3	Serial Data Out
4	Request to Send In
5	Clear to Send Out
6	Data Set Ready Out
7	Signal Ground
8	Data Carrier Detect Out
12	Carrier Detect
13	Clear to Send
14	Transmit Data
16	Receive Data
18	Data Set Ready
19	Request to Send
20	Data Terminal Ready
22	Ring Detect
23	Speed

Marker Beep Output

The time marker beep output is available from a 3-position terminal block. The output is 600 Ohms balanced at +4 dBm nominal.

The marker beeps are enabled by the DIP switches located at the front of the 5300ET module.

External Reference Input

The external reference input loop bridges 75 Ohms. The input level must be 2 Vp-p 3 dB. The choice of 5 MHz or 10 MHz as the external reference is made by the 5 MHz/10 MHz jumper on the 5300MO module.

Reference Output

The reference output is 5 MHz at 2 Vp-p into 75 Ohms.

1.3.8 Calibration

The only part of the CSD-5300 unit requiring calibration is the 5300MO Master Oscillator module. Please refer to the 5300MO circuit description of this manual for further details.

1.4 Operation

The CSD-5300 Master Clock System Driver can be controlled from either the front panel, an RS232 interface or over the telephone line.

1.4.1 Front Panel Control

The front panel constitutes the simplest and most readily available operational control.

The outside portion of the front panel contains the 6-digit time display, the external reference LED and the impulse clock correction mode LED. The 6-digit time display is duplicated in the inside portion of the front panel, which also contains 11 control mode push buttons, each identified by a number, a plus and a minus selection LED and operation instructions.

To select any of the control modes, press the shift button at the same time as the control mode button. The outside display will then go off while the inside display will show the number corresponding to the control mode that has been selected and a cursor. The number ensures correct selection of the mode while the cursor indicates that the system is ready to accept new information. A 30 second period is available to enter new information. If during this period no information has been entered, the CSD-5300 unit will cancel the control mode and will revert to its original status. After selecting the new information, press <SHIFT/ENTER>, i.e. press the shift button at the same time as the enter key to enter the information and to end the control mode.

If an error is made when selecting new information, the error can be deleted by pressing <SHIFT/CANCEL>, i.e. pressing the shift and cancel buttons simultaneously. This will cancel the control mode also but it will not affect any information previously contained in the unit.

On power-up, the two front panel displays and the impulse clock correction mode LED will flash. This indicates that no time information has been provided to the CSD-5300 unit. Upon entering the time, the flashing will stop.

The control modes operate as follows:

Input Time

The Input Time button is the first control mode of the inside panel. It is used to manually set the time of the unit. Upon selecting this mode, a cursor and the number 2 (corresponding to this mode) should appear in the inside display. The time is then entered in hours, minutes and seconds by pressing the buttons corresponding to the desired numbers.

Two options for synchronizing the CSD-5300 unit to the new time are available:

1. The first option consists in simply pressing <SHIFT/ ENTER> after the new time has been selected. The unit will start operating with the time provided at the instant the enter button is pressed.
2. The second option is provided for customer applications. It uses the external strobe input from pin 20 of the Auxiliary Output Connector located at the back of the CSD-5300 unit. The strobe input detects an external contact closure (active low). When said closure occurs, the clock will switch to the time provided.

Input Date

The next control mode is the Input Date mode. The date is selected as year, month and day in the same manner as for the Input Time mode.

This mode also allows inspection of the date contained in the CSD-5300 unit prior to selecting a new date. Approximately 3 seconds after selecting this mode, the cursor and the number 3 will go off, and the date contained in the unit will be shown on the inside display. If the existing date is adequate, press <SHIFT/CANCEL> to end the mode without changing the date.

Input Impulse Clock Reading

The Input Impulse Clock Reading mode is the next control mode of the inside panel. This mode is used to eliminate any discrepancy between the readings of the CSD-5300 unit and the impulse clocks connected to it. Upon selecting this mode, the impulse clocks are stopped. The time reading of the impulse clocks is then selected and entered in the same manner as for the Input Time mode. If there is a discrepancy between the readings, the impulse clock correction mode LED of the front panel will light steadily. This will indicate that the unit is acting to correct the discrepancy. The correction mode is carried out by either operating the impulse clocks at twice their normal speed or by stopping them until the time discrepancy is eliminated, whichever is faster. Once the time discrepancy is eliminated, the LED will go off and the clock drive will return to its normal speed.

In the case that no impulse clocks are connected to the clock driver, the impulse clock correction mode LED can be disabled by means of the DIP switch S7 located at the front of the 5300ET module. Switch S7 also stops any impulse clock connected to the unit.

Time Offsets

The next four control modes are time offsets. The first button is used for two offset modes, i.e. the hours, minutes and seconds offset and the auxiliary offset. To select either offset, DIP switch 1 located at the front of the 5300ET module should be set accordingly. To select the HMS mode, ensure that DIP switch 1 is its UP position.

This mode is basically used for leap seconds and for the spring and fall daylight saving/standard time change. Upon selecting this mode and before entering the time offset, selection of the plus or minus control should be made. This is done by pressing the shift button at the same time as the plus/minus button until the desired selection is made. The selection is then entered by pressing <SHIFT/ENTER>. Afterwards, the time offset is selected in the same manner as for the Input Time. The maximum offset allowed is 23 hours, 59 minutes, and 59 seconds.

Two options are available for implementing this offset. The change can be carried out immediately or it can be programmed to occur at any given time, e.g. at 3 AM when most time changes take place to avoid disruptions. To implement the change immediately, press <SHIFT/ENTER> and the offset will be carried out instantaneously. If a delay is desired, select the delay in hours, minutes and seconds and press <SHIFT/ENTER> and the offset will occur at the time selected.

The next control mode, that is the auxiliary offset, is used in applications where it is desired to show the time of a given time zone on one set of clocks and that of its time reference on another set of clocks. The auxiliary offset requires the use of clocks such as the LEITCH DAC-5000 Series which accept Time Code which has a user programmed constant offset inserted as user bits in the time code. Please refer to the Configuration of the Time and Control Code section of this manual for further details.

To select this mode, DIP switch 1 located at the front of the 5300ET module should be in the DOWN position. The mode is then selected in the same manner as the HMS offset with the exception that the auxiliary offset is done in 30-minute increments and the maximum offset allowed is 12 hours. The offset is implemented immediately.

The next control mode is the millisecond offset. This mode allows the clock to change instantaneously from 0 to 999 ms and is selected in the same manner as the hours, minutes and seconds offset. The change, however, is implemented immediately. This offset is basically used to synchronize the CSD-5300 unit to the beep tones of an external time transmission. If, for instance, the unit has an offset of half a second, diminishing offsets can be selected until it becomes synchronized with the time signal.

The fourth control mode provides an offset for the telephone line. This offset is basically used when the CSD-5300 unit is located in a Time Zone other than that of the Reference Standard from which the unit is updating its time via the telephone. If the time difference between the two locations is known, the unit can be programmed to subtract/add this time difference from the time received, so that the clock will maintain local time accurate to the Reference Standard Time.

Upon selecting this mode and before entering the offset, selection of plus or minus should be done and then the <SHIFT/ENTER> buttons pressed. Afterwards select the offset in hours, minutes and seconds and press <SHIFT/ENTER>. Then select the milliseconds offset and again press <SHIFT/ENTER> to end the control mode.

The CSD-5300 unit is also capable of automatically measuring loop-back delay and compensating for propagation delays through telephone lines and satellite telephone links. In cases where the propagation delay is known, it can be provided to the unit by entering a millisecond value to the Input Phone Offset mode and thus the correction will be done manually. It should be pointed out that when any value other than zero is entered, the automatic measuring of the loop-back delay and compensation capability of the unit will be disabled.

Phone Now

The last control mode of the inside panel is the Phone Now button. This control is used for setting up the CSD-5300N unit for the first time or to verify the accuracy of the display.

Upon selecting this mode and pressing <SHIFT/ENTER>, the unit will initiate an internal test diagnostics. If the test diagnostics is successfully completed, the unit will automatically dial the telephone number of the external standard. For details on how to input a telephone number, please refer to the Input New Telephone Number section of this manual. Once the external standard has been accessed, the time obtained and the unit reset itself, the new time will be immediately shown on the front display.

If, for whatever reason, the call is not successfully completed, the two front panel displays will flash to indicate that a new call is required. This will also create a P code in the Send Status function of the user mode. For further details, please refer to the User Mode section of this manual.

Whenever the Phone Now mode is selected, the call day counter for the automatic phone calls (please refer to the Input New Telephone Number section of this manual) will be reset.

1.4.2 RS232 and Telephone Line Control

The CSD-5300 Master Clock System Driver can also be controlled from either the telephone line or an RS232 interface. The RS232 interface may also be used to allow a computer to get time data from the unit. The unit is configured as a data set that plugs directly into video terminals at 300 baud, no parity, one stop bit. The telephone line capabilities are identical to the RS232 protocols with slight exceptions which will be described later.

The video terminal is normally connected locally for diagnostic use, time setting and setting up the characteristics of the unit. The telephone line, on the other hand, is basically used by third parties to obtain the time.

Two basic modes of RS232 and telephone line access are available. These are the user mode and the system mode.

1. User Mode

Whenever the RS232 interface is connected, the CSD-5300 unit is automatically in the user mode. This mode allows access to five basic functions. It also includes a HELP menu which details the commands for the five basic functions. The menu is accessed by typing HELP and then pressing the carriage return. The following will appear on the screen:

```
T    (CR) »  SEND TIME
D    (CR) »  SEND DATE
L    (CR) »  LOOP BACK
HU   (CR) »  HANG UP
S    (CR) »  SEND STATUS
```

The first function provides the time, the second provides the date, the third allows calculations of path delay if an external system is being called, the fourth disconnects the telephone line and the fifth provides the status of the unit. The five basic functions are accessed as follows:

Send Time function; type **T**, press carriage return and the time is sent to the terminal. Refer to the diagram below for the time sequence. The diagram shows the time request from the external device and the response of the CSD-5300 unit. Second boundaries are shown as /.

The time information is sent starting with a carriage return, timed so that the stop bit ends at the start of the next second. This is sent at the end of the second in which the time was requested. The time information is sent for three consecutive seconds in the following format. At the start of the second, the time of the next second is sent as HHMMSS. At the end of the second a carriage return is sent, timed as described above. This allows the carriage

return to function as a cue for the time information. After sending the time, the unit returns to user mode.

/Time Request CR/ HHMMSS CR/ HHMMSS CR/ HHMMSS CR/

Time Request Diagram

- **Send Date function**: type **D**, press carriage return and the date is sent once to the terminal. The date is sent in the format YYMMDD and is followed by a carriage return. After sending the date, the unit returns to user mode.
- **Loop Back function**: type **L**, press carriage return and the CSD-5300 unit echoes any character sent to it and then returns to user mode. The loop delay can be calculated since the character that was sent would return after twice the path delay.
- **Hang Up function**: in the case the unit is connected to the telephone line, type **HU** and press carriage return and the unit will hang up the telephone.
- **Send Status function**: type **S**, press carriage return and the status will be sent to the terminal. There are four different codes to indicate the status of the CSD-5300 unit. G indicates that the unit is operating properly, D that the internal test diagnostics have failed, T that the unit has not been provided with the time and P that the last phone update failed.

The user mode has a 30 second time out when accessed via the telephone line. If after 30 seconds no valid commands have been entered, the CSD-5300 unit sends the time three times and then hangs up. In addition to protecting the unit from outside sources attempting to break in, the 30 second time out allows units with different levels of complexity to take advantage of this service. For instance, a computer with a basic modem which is not capable of using the full protocol can wait for the time out period and then receive the time. Other systems with a greater level of complexity can use the commands, calculate the loop delay and get the time with much greater accuracy.

2. System Mode

The second basic mode of RS232 and telephone line access is known as the system mode. This mode allows access to the time setting capabilities of the CSD-5300 unit and will duplicate all of the functions of the front panel. In order to protect the unit against unwanted calls accessing and/or modifying the information contained in the unit, a password is required for RS232 access of the system mode. For telephone access, in addition to the password, the DIP switch S3 located at the front of the 5300ET module has to be enabled. The password consists of two parts. The first part is the word LEITCH. The second part is the serial number of the unit. The serial number of the unit consists of the year that the unit was manufactured plus a four digit number which is the individual number of the unit. This has the advantage that the password can be easily read from the front panel. Another advantage is that LEITCH Video, at

the request of the owner, is able to program the unit and run the test diagnostics program via the telephone. The owner can disable access to the unit by turning off the system access enable switch S3 of the 5300ET module.

To access the system mode, type LEITCH, press carriage return, type the serial number of the unit and press carriage return again. As with most computer systems the password is not echoed on the screen. A system mode prompt with the following message will appear on the display:

```
type HELP (CR) for menu
```

The following is the first question that appears:

```
do you want line feeds, yes, no?
```

This is provided for both intelligent and semi-intelligent video terminals and systems, some of which insert their own line feeds. For a basic system that inserts no line feeds, the answer is “yes”.

Typing **`help`** and pressing carriage return will bring up the command menu. There are seventeen functions in the command menu. Each command is identified by a code on the left hand side of the screen, followed by a carriage return (CR) when required and a description of the command.

The following will appear on the screen:

```
M2          (CR)  »   INPUT NEW TIME
M3          (CR)  »   INPUT NEW DATE
M4          (CR)  »   IMPULSE CLOCK TIME
M5          (CR)  »   HOURS, MIN., SEC. OFFSET
M6          (CR)  »   MILLI SEC. OFFSET
M7          (CR)  »   TELEPHONE (HMS & MILLI SEC.)
AUX         (CR)  »   AUXILIARY OFFSET
PHONE#      (CR)  »   INPUT NEW PHONE NUMBER

HELP        (CR)  »   GIVES THIS MENU
TEST        (CR)  »   SELF DIAGNOSTICS
QUIT        (CR)  »   BACK TO USER MODE
HANGUP      (CR)  »   HANG UP TELEPHONE LINE
LF          (CR)  »   LINE FEEDS (Y/N)

P                     PLUS
M                     MINUS
C                     CANCEL
(CR)                  ENTER
```

The first six of the functions are identical to those of the front panel and operate in a very similar manner. To select any of the functions, first type its corresponding code and then, where indicated, press carriage return. Selection of the different functions is as follows:

Input Time

The Input Time function is the first available command of the help menu. To select this function type **M2** and press carriage return. A prompt will appear on the screen that reads:

```
ENTER NEW TIME

 HH MM SS
```

The time is then typed in hours, minutes and seconds and the carriage return pressed afterwards. If a typing error is made, press **C** (Cancel) and the error will be eliminated. However, to re-enter the time, the Input Time function has to be selected again.

As in the case of the front panel, two options for synchronizing the unit to the new time are available.

1. The first option consists in simply pressing the carriage return after the new time has been typed. The unit will start operating with the time provided at the instant the enter button is pressed.
2. The second option uses the external strobe input of the Auxiliary Output Connector to switch to the time provided in the same manner as described for the front panel.

Input Date

The next function is the Input Date command. To select this function type **M3** and press carriage return. A prompt will appear on the screen that reads:

```
CURRENT DATE                ->(date contained in the unit)
ENTER NEW DATE              ->YY MM DD or CR
```

If the current date contained by the unit is acceptable, press carriage return and the message `EXIT DATE MODE` will appear on the screen. This indicates that the unit is back to system mode, and that the date has not been changed. If it is desired to alter the current date, type the new date as year, month and day and press carriage return. Again, a message showing the new date and the `EXIT DATE MODE` will appear on the screen to indicate that the change has been recorded and that the unit is back in system mode.

Input Impulse Clock Reading

The Input Impulse Clock Reading function is the next command of the menu. To select this function type M4 and press carriage return. A prompt will appear on the screen that reads:

```
ENTER TIME ON IMPULSE CLOCKS

HH MM SS
```

As in the case of the front panel, the impulse clocks connected to the unit will stop upon selecting this function. The time reading of the impulse clocks is then typed and the carriage return pressed in the same manner as for the Input Time function. If there is a discrepancy between the readings, then the impulse clock correction mode LED of the front panel will light steadily to indicate that the unit is acting to correct this discrepancy. As for the front panel, the correction mode is carried out by either operating the impulse clocks at twice their normal speed or by stopping them until the time discrepancy is eliminated, whichever is faster. Once the time discrepancy is eliminated, the LED will go off and the clock drive will return to its normal speed.

Time Offsets

The next four functions are time offsets and they operate as described for the front panel.

The first function is the hours, minutes and seconds offset. It is selected by typing **M5** and then pressing the carriage return. The following prompt will appear on the screen:

```
ENTER HMS OFFSET & TO OCCUR

 M/P & HH MM SS AT HH MM SS
```

First, selection of plus or minus is made. Type either P or M, as desired, and press carriage return. Then select the offset in hours, minutes, and seconds and press carriage return. The maximum offset allowed is 23 hours, 59 minutes, and 59 seconds as for the front panel.

Two options are available for implementing the offset. The change can be carried out immediately or it can be programmed to occur at any desired time.

To implement the change immediately, press the carriage return and the offset will be carried out instantaneously.

If it is desired to program the change at a given time, type the time in hours, minutes and seconds and then press the carriage return. The offset will occur at the time selected.

The next function is the millisecond offset. To select this function type **M6** and press carriage return. The following prompt will appear on the screen:

```
ENTER MILLI SEC OFFSET

M/P & MMM
```

Selection of plus or minus is made by again typing P or M, as desired, pressing the carriage return and then typing the desired offset (max. 999 ms) and pressing carriage return.

The third function provides an offset for the telephone line. To select it, type M7 and press carriage return. The following prompt will appear on the screen:

```
ENTER PHONE OFFSETS M/P & HH MM SS

 & MMM
```

Again selection of plus or minus, hours, minutes, seconds, and milliseconds is made as previously described.

The next function is the auxiliary offset. It is selected by typing AUX and pressing carriage return. The following message will appear:

```
ENTER AUX OFFSET (IN 30 MIN STEPS)

 M/P & HH MM
```

Selection of plus or minus and then the offset in 30-minutes increments and up to 12 hours is made as previously described.

Input New Telephone Number

The next function is the Input A New Phone Number. The objective of this function is to allow several units to be arranged in a hierarchical system; i.e. a reference unit connected to a Cesium standard which can provide a standard time to several local units.

To select this function type **PHONE#** and press carriage return. A prompt will appear on the screen that reads:

```
CALL DAY » XX
```

This message requests the desired frequency of calls to the reference unit in number of days. If the existing number of days is adequate, press carriage return. If it is desired to modify it, select the new number, press carriage return and the change will be recorded. Obviously, if zero is selected as the number of days, the unit will never call the reference unit.

After the call day has been entered, the following prompt will appear on the screen:

```
CALL TIME -> XX XX XX
```

This message requests the time of the day in which the call is to be made. If the existing time of the day is adequate, press carriage return. If it is desired to modify it, select the new time in hours, minutes and seconds, press carriage return and the change will be recorded. Normally this can be set for the middle of the night when telephone trunks are more readily available and calls are cheaper. If there is no answer, e.g. the trunk is not available or the unit to which the call is being made is busy, it will hang up and wait a random period of time before recalling. A total of seven attempts will be made to contact the unit. If after the seventh attempt no contact has been made, the unit will indicate that the telephone update has failed by sending a P code to the Send Status function of the user mode. It will also reset the call day counter and therefore will wait the existing number of days before recalling again.

In the case of a power failure, the unit, after waiting for a period of 20 minutes to allow the crystal oscillator oven to warm, will phone automatically and reset the call day counter if the call day recorded is not equal to 00 days.

After the call time has been recorded, the following prompt will appear on the screen:

```
PHONE # -> XXXXX
```

This message requests for a telephone number. If the existing number is acceptable, press carriage return and the number will be kept. If a new telephone number is desired, type the new number and press carriage return. The unit will accommodate both dial pulse and DTMF as well as the delay required for a PBX to obtain an outside line. Three different codes are available to indicate the type of dial and the delay. These are P for pulse, T for touch tone and D for delay. To enter a new phone number, first indicate the type of dial, P or T. After, for instance, entering a P it will remain in pulse mode until a T is entered.

As an example, enter P1 T416 4459640. This would have the effect of pulsing a 1 and then dialing in DTMF the area code and the remaining seven numbers. If a PBX is available and, for example, it is desired to access an old model that accepts pulse only, P9 can be entered which will give pulse 9 for an outside line, then D3 which will provide a delay of 3 seconds for obtaining an outside line and then T followed by the number to call.

The phone number input routines will accept spaces and dashes. These can be entered to format the output so that the phone number is easily readable on the screen. The total number of characters of a phone number input routine, including T, P, and D, is twenty five.

System Mode Menu

The next command is the System Mode Menu function. When typing **HELP** and pressing carriage return, the system mode menu will appear on the screen.

Self Diagnostics

The next command of the system mode menu is the self diagnostics function. When typing TEST and pressing carriage return, the unit will enter a diagnostics cycle. The diagnostics cycle is the same to that performed when the unit calls an external source or on power up. The following will appear on the screen:

```
EEPROM TEST->    PASSED (or FAILED)

RAM TEST   ->    PASSED (or FAILED)

PGM TEST   ->    PASSED (or FAILED)

MODEM TEST ->    PASSED (or FAILED)

DIAGNOSTICS DONE.....
```

In the case the test diagnostics fail, please contact LEITCH's Service Department.

Back To User Mode

The Back To User Mode function is the next command of the system mode menu. When typing QUIT and pressing carriage return, the unit will return to the user mode.

Hang Up the Telephone

The next command of the menu is the Hang Up The Telephone Line function. When typing HANGUP and pressing the carriage return, the unit will hang up the telephone and will return to the user mode.

Line Feeds

The next command of the system mode menu is the Line Feeds function. When typing **LF** and pressing carriage return, the following message will appear on the screen:

```
DO YOU WANT LINE FEEDS? (Y/N) » Y or (N)
```

This command will alter the information provided when first accessing the system mode.

Miscellaneous Commands

Four other commands are available in the system mode menu. These are

- C for cancel,
- CR for enter,
- P for plus, and
- M for minus.

When selecting any of these commands, it is not required to press carriage return. The commands are self-explanatory; therefore no further details are provided.

Set Window

The Set Window function is not included in the system mode menu due to the fact that if these values are assigned incorrectly, all outgoing telephone calls would fail. All units are pre-programmed with the default prior to delivery.

The purpose of this function is to attempt to detect asymmetrical path delays when an external system is being called i.e. a call being placed via satellite in one way and via land line on the other. All calls received with a delay that falls within the values set by the window will automatically be rejected.

To access this function, type **`SET`** and press carriage return. The prompt `WHAT?` will appear on the screen. The purpose of this message is to protect the unit against unwanted modifications of the default. Then type **`WINDOW`** and again press carriage return and the following will appear on the screen:

```
*************** WARNING ***************

* IF DONE INCORRECTLY ALL OUTGOING   *

*     PHONE CALLS WILL FAIL          *

*****************************************

ILLEGAL DELAY WINDOW IS BETWEEN XXXX AND XXXX

ENTER LOWER VALUE IN XXXX MILLI SEC.

»
```

Select the lower value of the window and then press the carriage return. If the existing value is adequate simply press carriage return and the value will be maintained.

Then, the following prompt will appear on the screen:

```
ENTER UPPER VALUE IN XXXX MILLI SEC.

»
```

The upper value of the window is then selected as previously described for the lower window, and the following will appear on the screen:

`ILLEGAL DELAY WINDOW IS BETWEEN` (new values selected)

```
EXIT DELAY WINDOW MODE
```

This message will indicate the new values contained by the unit and that this function is completed.

Autochange / Normal Mode Selection

DIP switch 8 at the front of the 5300ET module selects either the Autochange Mode when set in the up position or the Normal Mode of operation when set in the down position.

The Autochange Mode is selected in cases such as whenever a Clock Autochange system is used with two CSD-5300 drivers to provide continuity of impulse drives, time code signals, etc. In the case of a malfunction to the assigned Master Driver, the Clock Autochange will switch from one driver to the other. When the Clock Autochange Mode is selected, the success or failure of a telephone call to be carried through will not affect the Time Valid Line.

When the Normal Mode is selected, the success or failure of a telephone call to be carried through will affect the status of the Time Valid Line.

1.5 Operation Summary

1.5.1 Front Panel

The front panel constitutes the simplest and most readily available operational control. The following functions are available:

Input Time	Press SHIFT/Input Time buttons simultaneously. Select the time in HH MM SS. Press<SHIFT/ENTER> to instantaneously input new time or strobe pin 20 of the Auxiliary Output Connector to synchronize the new time to an external source.
Input Date	Press SHIFT/Input Date buttons simultaneously. Inspect date of unit. If adequate, press <SHIFT/CANCEL> to end function. To alter existing date, select date in YY MM DD and press <SHIFT/ENTER>.
Input Impulse	Press the SHIFT/Input Impulse Clock Reading buttons simultaneously. Enter the readings of Clock Reading the impulse clocks and press <SHIFT/ENTER>.
HMS Offset	Set DIP switch 1 at front of 5300ET in the UP position. Press the SHIFT/HMS Offset buttons simultaneously. Select P or M and simultaneously press the SHIFT button. Press <SHIFT/ENTER>. Then select the offset (max. 23 h. 59 m. 59 s). To implement the offset instantaneously, press <SHIFT/ENTER>. If to occur at a certain time, enter the time and press <SHIFT/ENTER>.
Auxiliary	Set DIP switch 1 at front of 5300ET in the DOWN position. Press the SHIFT/AUX Offset buttons simultaneously. Select P or M and simultaneously press the SHIFT button. Press <SHIFT/ENTER>. Then enter the offset (in 30 minute increments and max. 12 h) and press <SHIFT/ENTER>.
Milliseconds	Press the SHIFT/Millisec Offset buttons simultaneously. Select P or M and simultaneously press the Offset SHIFT button. Press <SHIFT/ENTER>. Then enter the offset (0 to 999 ms) and press <SHIFT/ENTER>.
Telephone	Press SHIFT/Telephone Offset buttons simultaneously. Select P or M and simultaneously press the SHIFT Offset button. Then press <SHIFT/ENTER>. Enter offset & press <SHIFT/ENTER>. Select millisec offset & press <SHIFT/ENTER>
Phone Now	Press SHIFT/Phone Now buttons simultaneously, then <SHIFT/ENTER>. Upon completing the test diagnostics, the unit will automatically dial the telephone number provided. Please refer to System Mode section for details to input phone. To cancel this function, press <SHIFT/CANCEL>.

1.5.2 RS232 And Telephone Line Control

User Mode

Whenever the RS232/telephone interface is connected, the unit is automatically in User Mode. The following functions are available in this mode:

Send Time	Type T and press CR. The time will be provided for three consecutive seconds.
Send Date	Type D and press CR. The date will be provided once.
Loop Back	Type L and CR. The next character selected will be echoed.
Hang Up	Type HU and CR. The unit will hang up the telephone.
Send Status	Type S and CR. The status will be sent to the terminal.

System Mode

To access the System Mode, type LEITCH, press CR, type the serial number of the unit and press CR. The following functions are available:

Line Feeds	Type LF and press CR. The message 'Do you want line feeds' will appear on the screen. Type Y for basic systems and N for systems which insert their own line feeds and then press CR.
Help Menu	Type HELP and press CR. The system menu will appear on the screen.
Input Time	Type M2 and press CR. The message, Enter New Time -> HH MM SS, will appear. Type the desired new time and press CR to input the time instantaneously or strobe pin 20 of the Auxiliary Output Connector.
Input Date	Type M3 and press CR. The message, Current Date -> YY MM DD Enter New Date » YY MM DD or CR, will appear. If the existing date is acceptable, press CR. If desired to change, type the new date and press CR.
Input Impulse Clock Reading	Type M4 and press CR. The message, Enter Impulse Clock Time » HH MM SS Clock Reading, will appear. Select the time and press CR.
HMS Offset	Type M5 and press CR. The message, Enter HMS Offset » M/P & HH MM SS & Time to Occur at HH MM SS, will appear. Select P or M press CR, type the offset (max. 23 hours, 59 min. and 59 sec.), press CR and either press CR to implement the change immediately or select the time when the change is to occur and press CR.
Milliseconds	Type M6 and press CR. The message, Enter Milli Sec Offset » M/P & MMM Offset, will appear. Select P or M, press CR, type offset (max. 999ms) and press CR.
Phone Offset	Type M7 and press CR. The message, Enter Phone Offset » P or M & HH MM SS & MMM, will appear. Select P or M press CR, type offset, press CR, type milliseconds offset and press CR.
Auxiliary	Type AUX and press CR. The message, Enter Aux Offset (in 30 min steps) » P or M & HH MM, will appear. Offset Select P or M, press CR. Then select the offset in 30-minute increments (max. 12 hours) and press CR.
Input New Phone Number	Type PHONE# and press CR. The message, Call Day -> XX, will appear. If the existing Phone number is adequate, press CR. If desired to change it, type the new number and press CR. The message, Call Time » HH MM SS, will then appear. If the existing time is adequate, press carriage return. If desired to modify it, type new time and press CR. Then, the message, Phone # » XXXXXX, will appear. If the existing number is adequate press CR. If desired to change it, type the new number (max. 25 characters) by indicating the type of dial (P for pulse and T for touch tone) and, if required, a delay in seconds (D and up to 9 sec.) Spaces and dashes are allowed.
Self Diagnostics	Type TEST and press CR. The unit will perform a diagnostics cycle and the results will appear on the screen.
Back to User Mode	Type QUIT and press CR. The unit will return to the User Mode.
Hang Up	Type HANGUP and press CR. The unit will immediately hang up the telephone.

1.6 Configuration of the Time and Control Code

1.6.1 SMPTE Serial Time Code

The SMPTE Serial Time Code contains the time of the day in hours, minutes and seconds. Since time code was originally intended as a timing and control code for video tape recording, each second is divided into thirty equal parts that coincide with the picture frames of the associated video signal. Thus, each frame can be identified by a unique and complete code address. The time code output of the CSD-5300 is intended only to convey time-of-day information but a frame count is still included. Note that the time code output of the CSD-5300 is non-drop-frame and real time, not color time, and cannot be locked to a video signal.

Code Format

Each code address consists of eighty bits, numbered 0 through 79. Each address starts at the clock edge before the first address bit (bit zero) which corresponds to the beginning of Line 5 in Fields I and III, as defined in EIA Standard RS170A.

The eighty bits of a code address are assigned as shown in Figure 1-1 on page 1-34 and grouped as follows:

- Eight binary groups consisting of 32 spare user bits.
- Eight time address groups consisting of 28 assigned addresses and four unassigned addresses (all unassigned bits are zeros).
- One synchronizing word consisting of sixteen bits.

The time address groups and the binary groups are arranged alternatively. This is to distinguish the information of a given combination of groups from that of the synchronizing word, which has a typical structure of twelve successive logic ones. If groups of the same type were together, it would be necessary to assign fixed zeros to two of the thirty two bits to prevent an occasional generation of a synchronizing word within the groups. This would reduce the available number of bits to thirty.

The binary groups are intended for storage of user’s supplementary data in any fashion and without restrictions.

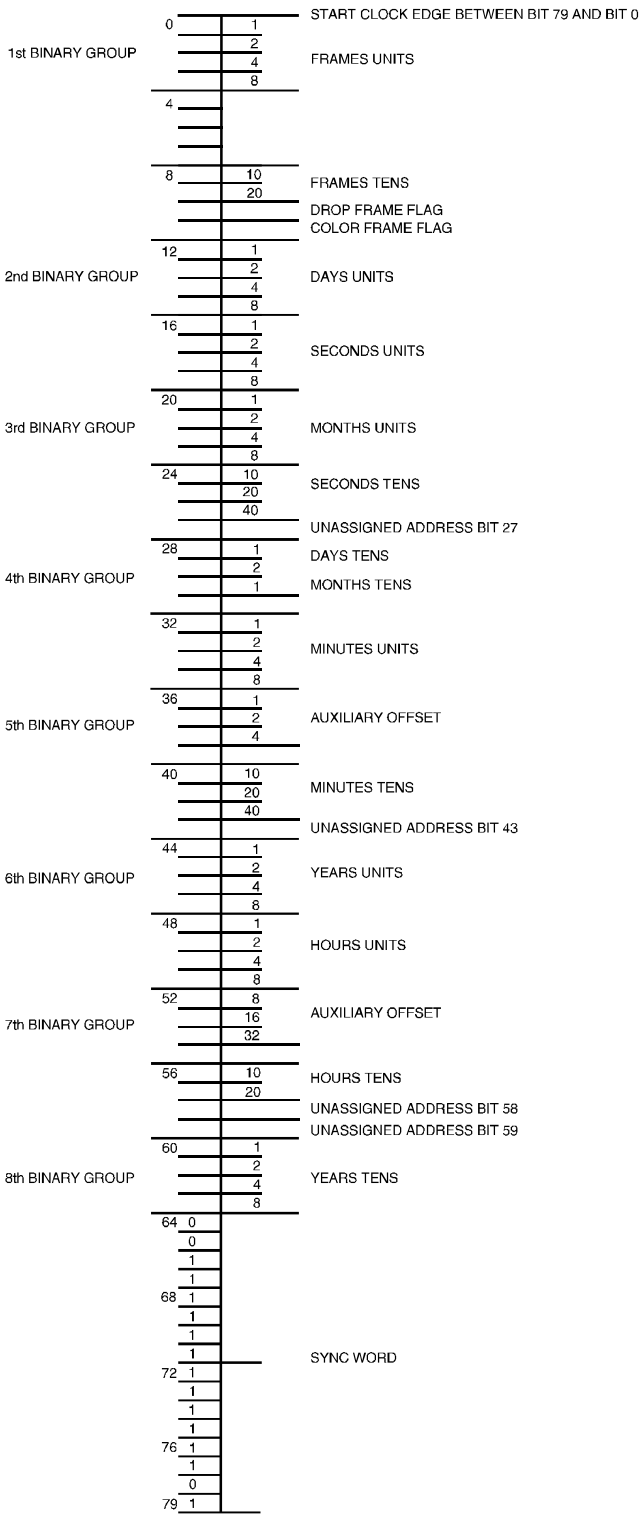


Figure 1-1: Assigning the eighty bits of a code address

The time address groups use the 24-hour clock system and are based upon the Binary Coded Decimal (BCD) system. Conservation of bits is achieved due to the fact that the count of some addresses does not reach to 9 and, therefore, 4 bits are not always required.

1.6.2 Composition of the Time Address

The eight time address groups (see Fig.1) are arranged as follows:

Units Frames:	Bits 0-3; 4 bit BCD arranged 1, 2, 4, 8. Count 0-9.
Tens Frames:	Bits 8-9; 2 bit BCD arranged 1, 2. Count 0-2.
Unit Seconds:	Bits 16-19; 4 bit BCD arranged 1, 2, 4, 8. Count 0-9.
Tens Seconds:	Bits 24-26; 3 bit BCD arranged 1, 2, 4. Count 0-5.
Units Minutes:	Bits 32-35; 4 bit BCD arranged 1, 2, 4, 8. Count 0-9.
Tens Minutes:	Bits 40-42; 3 bit BCD arranged 1, 2, 4. Count 0-5.
Units Hours:	Bits 48-51; 4 bit BCD arranged 1, 2, 4, 8. Count 0-9.
Tens Hours:	Bits 56-57; 2 bit BCD arranged 1, 2. Count 0-2.
Units Days:	Bits 12-16; 4 bit BCD arranged 1, 2, 4, 8. Count 0-9.
Tens Days:	Bits 28-29; 2 bit BCD arranged 1, 2. Count 0-2.
Units Months:	Bits 20-23; 4 bit BCD arranged 1, 2, 4, 8. Count 0-9.
Tens Months:	Bit 30; 1 bit BCD. Count 0-1.
Units Years:	Bits 44-47; 4 bit BCD arranged 1, 2, 4, 8. Count 0-9.
Tens Years:	Bits 60-63; 4 bit BCD arranged 1, 2, 4, 8. Count 0-9.

The time address contains six reserved bits. Two of the bits, namely bit 10 and bit 11, are used for identification of the Drop Frame Flag and the Color Frame Flag. The remaining four bits, namely bits 27, 43, 58, and 59, are currently unassigned. Since the time code output of the CSD-5300 contains time-of-day information only, these six bits are set to zero.

The synchronizing word enables the reading device to set and control counters so that the originally encoded information can be retrieved. This makes the code self-contained.

1.6.3 Auxiliary Offset

If an auxiliary offset is in use, the value of the offset is contained in six of the user bits of the time code. In this way an auxiliary offset does not affect the time data as seen by standard time code readers. An auxiliary offset is encoded in 30-minute increments, to be added to the main time information contained in the time code. The CSD-5300 allows an auxiliary offset of up to 12 hours in either direction. For simplicity, this is encoded in the time code as an offset in the positive direction of up to 23 hours 30 minutes, or 47 half hour steps. This can be encoded in binary form in 6-bits. The information is split into two 3-bit groups. The 3 lower bits are encoded in bits 36, 37 and 38 of the time code, with bit 36 as the LSB. The 3 upper bits are encoded in bits 52, 53 and 54.

1.7 CSD-5300N System Schematic

Chapter 2

5300BH Batter Holder

2.1 Circuit Description

The 5300BH contains the batteries used to enable the CSD-5300 to keep time during a power failure. The 5300BH fits into the frame of the CSD-5300 just to the left of the 5300MB and 5300CD modules.

The 5300BH, as shipped, is configured for 3 nine volt alkaline batteries. These batteries will keep the unit running for over 8 hours in the event of a power failure. Provision is made for the use of rechargeable batteries.

With reference to the circuit diagram, the batteries are isolated by diodes D2, D4 and D6. These diodes are required because the +9B rail is fed with 13 volts by the 5300PS power supply when either 117VAC or 24VDC is present. When power is present, these diodes are reverse biased and prevent any current flow into the batteries. When power is removed, the diodes are forward biased by the batteries and allow current to flow to the processor circuitry.

The regulators feeding the processor circuitry require approximately 6 volts to operate. Diodes D2, D4, and D6 have a forward drop of approximately 0.7 volt. As a result, the processor circuitry will continue to operate until the battery voltage falls below about 6.7 volts. The 12 ohm resistor provides short circuit protection for the diodes.

Diodes D1, D3, and D5 are factory installed to allow use of rechargeable batteries. If rechargeable batteries are used, the 3 resistors shown on the schematic may be added to allow charging of these batteries. If resistors are installed, diodes D1, D3 and D5 will be forward biased when 13 volts is applied to the +9B rail and the resistors will set the charge rate.

The resistor value should be chosen to set the desired trickle charge rate based on the amp hour rating of the battery, the wattage rating of the resistor, and a supply voltage of approximately 13 volts.

2.2 5300BH Battery Holder Schematic

Chapter 3

5300CA Control Assembly Module

3.1 Circuit Description

The 5300CA Control Assembly contains LED displays and a keyboard to allow front panel control of the CSD-5300. The 5300CA appears to the asynchronous processor on the 5300ET module as a memory-mapped peripheral occupying 8 consecutive addresses.

3.1.1 Processor Interface

The 5300CA accepts data from the processor for display and creates a strobe and key code whenever a key is pressed. The processor uses buffered signals from its data and address busses to communicate with the 5300CA module. Processor address lines A0 to A2 are connected to pins 5, 9 and 10 of the module connector J1. Processor data lines D0 to D3 and D7 are connected to pins 11, 4, 3, 12, and 2 of J1 respectively. The processor creates two signals to control the 5300CA circuitry. These are Board Enable Read' and Board Enable Write'. They are connected to pins 8 and 6 of J1 respectively.

3.1.2 Display Circuitry

The display controller IC1 drives the two front panel seven-segment displays. IC1 contains six registers which can be written to by the processor. These registers occupy the first six addresses on the board. To write to a register, the processor pulses the Board Enable Write line low. IC1 then reads the data on the data lines into the register selected by the address lines. Each register corresponds to a display digit. The first register (answering to the lowest address) corresponds to the leftmost digit of the display. IC1 will display the seven-segment equivalent of the binary codes in the registers. To display a blank, binary code 1111 is used. A fifth bit, corresponding to D7, is normally used in each register to drive the decimal point on each digit. In this circuit it is used to drive the discrete LEDs.

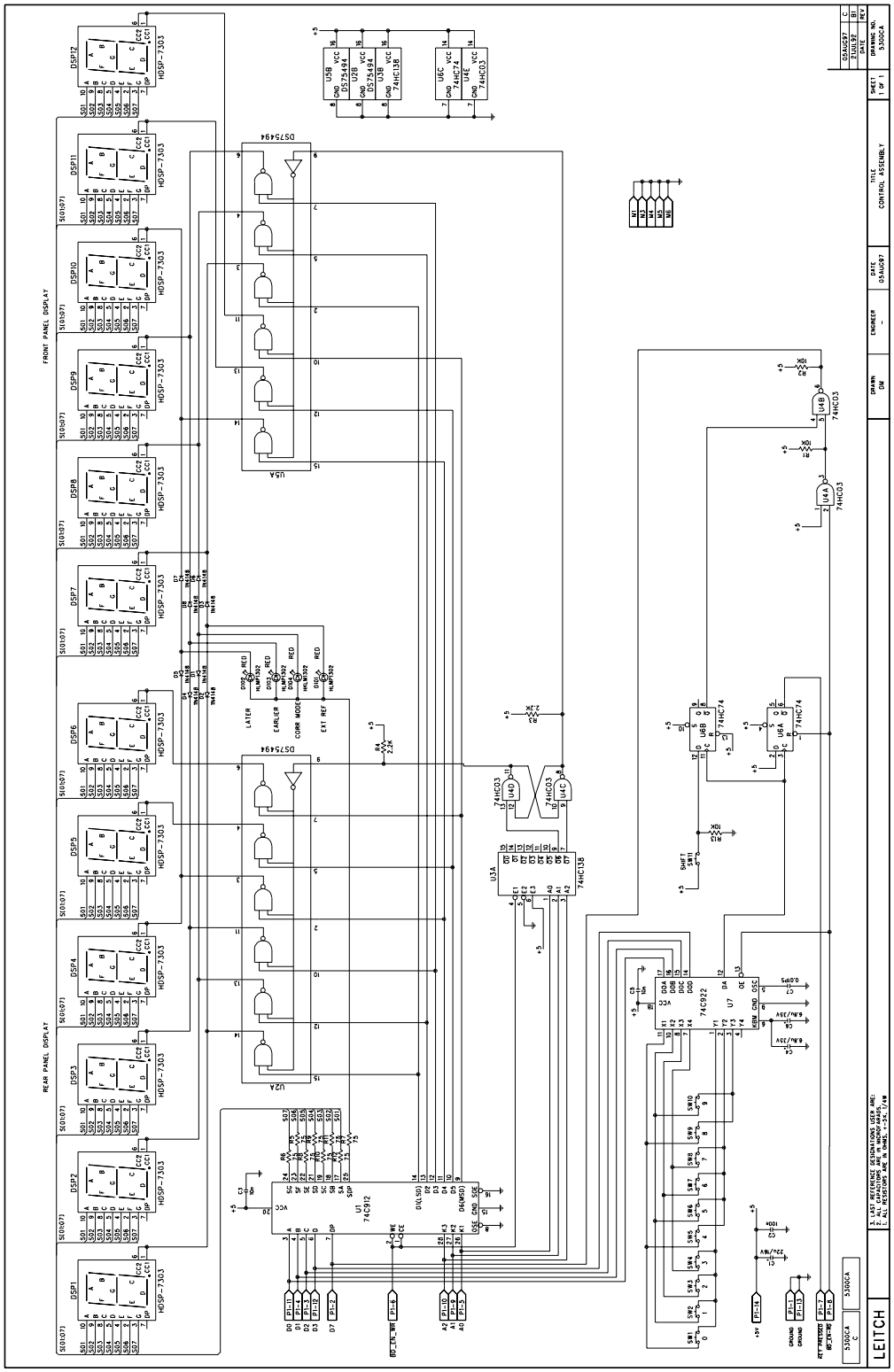
The LED drive output of IC1 is in multiplexed form. The digit drive signals require buffering to drive the displays. Two switchable buffers, IC2 and IC5, are used to allow two separate sets of displays to be driven. One of eight decoder IC3 is used to toggle the flip-flop formed by IC4C and D. Writing to the seventh address on the board causes a pulse from pin 9 of IC3 to toggle the flip-flop to enable the displays on the outside of the front panel. Similarly, writing to the eighth address toggles the output to enable the displays on the inside of the front panel.

The drive for each segment is paralleled to all the displays. The decimal point segment drive is used to drive the discrete LEDs. Two sets of four diodes, D1 to D8, are used to ensure that the discrete LEDs display the same information whether the outside or inside displays are selected.

3.1.3 The Keyboard Encoder

IC7, a 74C922, is a keyboard encoder. It scans an array of keys and generates a strobe and a binary code whenever a key is pressed. The capacitor on pin 5 of IC7 sets the scan rate, and the capacitors on pin 6 set the debounce time. When a key is pressed, the Data Available output, pin 12 of IC7, goes high. This clocks both halves of the dual D flip-flop IC6. The Q' output of IC6A generates the Key Pressed output strobe to the processor, and IC6B clocks in the state of the Shift key. The outputs of IC7 are tri-state and are connected to the data bus pins of the module connector J1. When the processor asserts the Board Enable Read line to get the key code, the outputs of IC7 are enabled to the bus, and the Key Pressed' strobe is reset. The state of the Shift key is gated onto the data bus by the open collector NAND gate IC4B

3.2 5300CA Control Assembly Schematic



Chapter 4

5300ET Electronic Timer Module

4.1 Circuit Description

The 5300ET Electronic Timer module is the control center of the CSD-5300 Master Clock System Driver unit. Two separate microprocessor circuits are contained in this module. These are named the synchronous and the asynchronous processors. The synchronous processor conducts most of the time keeping operations. It also generates the Time Code, the Serial Time Data, the Impulse Drive signals for the 5300CD Clock Driver module and the Parallel BCD Time. The asynchronous processor handles most of the front panel, telephone and RS232 interface control tasks.

An 8-position DIP switch mounted on the front of the 5300ET module allows selection of operational parameters.

4.1.1 System Clock

The 5 MHz clock from the 5300MO Master Oscillator module, enters the 5300ET module at pin A27. It is buffered by IC33E and IC43E and fed to the clock input of the synchronous and asynchronous processors respectively.

4.1.2 Memory Map

All support devices in both microcomputer systems are memory mapped. Two identical address decoding schemes are provided, one for each processor. Since the circuits are identical, only that for the synchronous processor will be described.

With the exception of the RAM I/O Timer IC18, the address location of each device is selected by the address decoder IC28, a 1 of 8 decoder. Inputs to IC28 are address lines 13, 14 and 15, the three most significant lines from the synchronous processor IC19 at pins 6, 7, and 8. This provides an address map based on 8000Hex byte divisions. The address decoder also uses the I/O Memory select line and the address latch enable line from IC19 at pins 34 and 30 respectively to determine when a valid address is present.

IC18 the RAM I/O Timer is selected by gate IC34B. Inputs to gate IC34B are address lines 14 and 15, the two most significant address lines of the synchronous processor IC19. Thus, IC18 will be selected at address C000Hex and above.

Memory Map

Synchronous Processor

0 - 1FFFH	IC20 Program EPROM
2000H - 3FFFH	IC25 Input Buffer, IC26 Serial Time Latch and ICs 24, 27, 30, and 36 Parallel Time Shift Registers
4000H - 5FFFH	Ring Detect Reset Pulse
6000H - 7FFFH	Synchronous Interrupt Reset Pulse
8000H - 9FFFH	Serial Time Latch Pulse
A000H - BFFFH	Spare
C000H - FFFFH	IC18 RAM I/O Timer

Asynchronous Processor

0 - 1FFFH	IC7 Program EPROM 1
2000H - 3FFFH	IC8 Program EPROM 2
4000H - 5FFFH	IC14 Control Assembly Interface
6000H - 7FFFH	IC2 Input Buffer 1 and IC13 Output Latch
8000H - 9FFFH	IC3 Input Buffer 2
A000H - BFFFH	Spare
C000H - FFFFH	IC6 RAM I/O Timer

4.1.3 Synchronous Processor

The synchronous processor IC19 is an 8-bit CMOS NSC800 Microprocessor. It is supported by IC18, an NSC810A RAM I/O Timer that provides 128 bytes of RAM, two 16-bit timers and input/output lines. The microprocessor data bus is multiplexed with the lower 8-bits of the microprocessor address bus. Address demultiplexer for the program EPROM IC20 is carried out by the 8-bit data latch IC21.

IC25 is configured as an input buffer. Its outputs are gated onto the data bus by the processor read pulse and the 2000Hex address select line which are combined in gate IC35C.

Timer 0 of the RAM I/O Timer IC18 is fed with 600 kHz from the 5300MO Master Oscillator module and produces a 4800 Hz pulse train. 4800 Hz corresponds to a period of 208 µs which is the edge rate of the SMPTE Time Code. The 4800 Hz line clocks output latch IC22 which is used to synchronize the time code, serial time, and the 1 Hz and 60 Hz outputs.

In order to generate SMPTE time code, the processor must decide every 208ms whether or not to create an edge of time code. Using the output latch IC22 to synchronize the time code output allows the processor to create the time code with relaxed timing constraints.

The 4800 Hz pulses are too short for the processor to catch by polling. Therefore, the pulses are fed to flip-flop IC29A whose output indicates to the processor when to create a new edge of time code via pin 5 of the RAM I/O Timer IC18. The processor creates a reset pulse for IC29A by reading or writing to address 6000Hex, thus preparing the flip-flop for the next pulse.

4.1.4 Serial Time Data/Clock

The serial time data stream is also provided by latch IC22 at pin 6. It presents the same data as the SMPTE Time Code but without the built-in synchronizing pulses. The output consists of BCD frame count, seconds, minutes and hours sent 30 times a second, least significant bit first. The serial data stream is accompanied by a serial time clock stream. The clock output rises at the start of each data bit time and falls half way through. Data output can be read at the falling edge of the clock.

Flip-flops IC26A and B are used in the creation of the data and clock streams. IC26A latches bit 0 of the processor data bus when it receives a clock impulse. The clock is provided by gate IC35D and consists of the write line from pin 31 of the processor gated with the 2000Hex select line of IC28. When the processor writes to address 2000Hex, IC26A latches the data on bit 0 of the data bus and sends it to pin 7 of the output latch IC22. IC26B receives the same clock signals and its output is fed to pin 8 of IC22 to create the serial time clock.

Since the bit period for the serial clock data is equal to twice the 208 µs clock of IC22, the serial time clock output of IC22 is fed to the reset input of IC26B. Consequently, when a high output from IC26B is latched 208 µs later through the output of IC22, it will reset IC26B. Thus, the serial time clock will be low during the second half of the serial time data bit period.

4.1.5 Parallel BCD Time Data

The serial time data is converted into parallel BCD time data by shift registers IC24, 27, 30 and 36. The clock for the shift registers is the same signal that clocks IC26A and B while bit 0 from the processor data bus is fed to the D

input of IC36, the first register of the shift register chain. Therefore, the registers clock the same data that the processor writes to IC26A. Data is latched in the registers by means of the serial time latch pulses from IC35A and inverter IC33D which provide the gated combination of the write pulse from the processor and address 8000Hex from IC28. The processor provides a latch pulse just before the end of each time code frame, so that the parallel time data remains valid for the entire frame, independent of the new data clocking through the shift registers. The serial time latch pulses are also sent to the CSD-5300 Auxiliary Output Connector via IC43D for use by external equipment.

4.1.6 1 Hz and 60 Hz/50 Hz Logic Levels

The synchronous processor circuitry also creates square waves at 1 Hz and 60 Hz/50 Hz. To maintain these outputs synchronous with the Time Code, they are fed through the synchronous output latch IC22.

4.1.7 Time Code Output

The time code output of IC22 is converted to a balanced feed by the output driver circuit. This circuit is composed of two identical output stages, each consisting of an inverter which drives a push-pull pair of transistors. The stage composed of IC1B, Q3 and Q4 receives the time code output directly while the section composed of IC1C, Q1 and Q2 receives the output inverted by IC1A.

The entire circuit is powered by IC37, a 5 Volt Regulator with a current limit of approximately 100 mA. This protects the output drivers from short circuits.

Two sets of outputs are provided, a 600 Ohm output through a pair of 301 Ohm 1% resistors and a low impedance output through a pair of 22 Ohm resistors.

4.1.8 Aural Time Markers

The synchronous processor circuit also provides aural time markers. These consist of one 300 ms burst of 1200Hz for the hour and two 300 ms burst of 1200 Hz separated by a 300 ms pause for the half hour.

The hour and half hour markers are enabled by switches S5 and S6 respectively at the front of the 5300ET module. These switches are read by the processor via input buffer IC25. During each burst, the tone present output at pin 33 of IC18 goes low.

To prevent DC offset shifts, the time tone and tone present pulses are added in 62 kΩ and 120 kΩ resistors respectively before being fed to IC44A. IC44A is arranged in a low-pass filter configuration which also forms half of the output driver stage. The output of IC44A is fed to IC44B which is connected as a

simple inverter which forms the other half of the output stage. In this manner a balanced output for the aural time markers is achieved.

The tone present signal is also buffered and inverted by IC15C and sent to the CSD-5300 Auxiliary Output Connector for use by external equipment.

4.1.9 Impulse Clock Drive

The synchronous processor circuit also creates the impulse clock drive signals. These are provided by pins 35 and 36 of IC18, buffered by IC15D and E respectively and sent to the 5300CD Impulse Clock Driver module. The 5300CD module provides impulse signal buffering to drive up to 25 clocks. It also detects overload or short circuit conditions on a pulse-by-pulse basis, and reports this status to the processor. The status information from the 5300CD module is sent back to pins 4 and 2 of the input buffer IC25. These inputs are high if the last impulse from the synchronous processor was successful and low if the output of the 5300CD module was shorted. The impulse clock drive is enabled or disabled by switch S7. This switch is located at the front of the 5300ET module and connected to pin 17 of the input buffer IC25.

When the impulse clocks are stopped by the synchronous processor, the Impulse Clocks Stopped output line from IC18 pin 31 is raised. This line is buffered through IC22.

When the 5300CD module is present, pin A6 of the 5300ET module is grounded (by a link to ground on the 5300CD board) and, consequently, pin 6 of IC25 is also grounded. This informs the synchronous processor whether the 5300CD module is present or not.

In the absence of the 5300CD module, the processor will create no impulse drive signals.

4.1.10 Ring Detection Circuit

Ringing activity is indicated by frequencies between 15 and 68 Hz on the telephone line. This is detected by the ring detection circuit of the 5300MB module.

The output of the detection circuit clocks the ring detection latch IC29B. Since the detection circuit doubles the frequency of the ringing voltage, frequencies in excess of 30 Hz must be detected as valid ringing.

The output of IC29B is sent to the synchronous processor via IC25. The processor reads, then resets IC25 30 times per second via address 4000Hex from IC28. Since the minimum ring detection time is half a second, 15 consecutive readings by the processor that are detected as a high at the output of IC29B will qualify as a valid ring. Ring detection can be enabled or disabled

by closing or opening switch S4. The switch S4 is located at the front of the 5300ET module and, when opened, will cause the output of IC29B to be high upon receiving an impulse clock from the ring detection circuit. When S4 is closed, the output will be low.

Upon detecting valid ringing, the synchronous processor will wait for 2 seconds to allow the ringing to cease before informing the asynchronous processor that a valid ring has been detected.

4.1.11 Watch Dog and Reset Circuit

Each of the two processors on the 5300ET module is provided with its own watch dog and reset circuit. The purpose of this circuit is to ensure clean startups when connecting power and to stop processor runaway due to power dips or any other type of disturbance.

The heart of the watch dog and reset circuit are voltage monitors IC31 and 32. These two circuits monitor the power supply voltage connected to their sensing input at pin 7 and reset the processor whenever that voltage falls below about 4.55 Volts. They also provide a power on reset pulse whose duration is dependent on the capacitor connected to pin 3, in this case a 22 µF capacitor. The voltage monitor will hold the processor reset line low for approximately 300 ms after the power supply has stabilized at 5 Volts and then will allow the processor to operate.

The periodic reset function of the watch dog timers is created by counting down the 600 kHz signal from the 5300MO Master Oscillator module. IC42, a multistage divider counts the 600 kHz down to 36.6 Hz. In the case of the synchronous processor, this signal is applied to IC40, another multi-stage divider. In the absence of processor activity, IC40 will provide a pulse every 3.5 seconds. This pulse is applied to one input of gate IC34C and provided that the watch dog disable test point connected to the other input of IC34C is not grounded, the output pulse will be sent, via inverter IC33B, to the reset input of IC31 which, in turn, will reset the synchronous processor. The active high reset output of the voltage monitor IC31 at pin 6 will also reset IC40 so that should the synchronous processor not become operational as a result of the reset pulse, another reset pulse will be created in 3.5 seconds.

The time code output from IC18 pin 29 indicates processor activity and can therefore be used to reset the watch dog circuit. The pulse output from IC18 pin 29 is differentiated by a 0.001 µF capacitor and a 20 kΩ and 10 kΩ resistor network and fed to the reset input of IC40 at pin 12. Since the repetition rate of the time code pulses is approximately 4800 Hz, IC40 will not create any reset pulses during processor activity.

The watch dog and reset circuit for the asynchronous processor consists of IC41 and IC32. It operates in exactly the same manner as that for the

synchronous processor. Processor activity pulses from the asynchronous processor are differentiated and applied to IC41 to reset the watch dog circuitry.

Since the +5B power supply to the synchronous processor is supplied by batteries when the AC power fails, the synchronous processor circuitry uses the absence of +5 Volts to detect when AC power has failed and uses this information to minimize power consumption while running on batteries. The +5 Volts fail information from IC32 is applied to inverter IC33F and fed to the output control line of the synchronous output latch IC22. When the +5 Volts fails, the output drivers on this latch are turned off, lowering the power consumption of the device. In a similar manner the +5 Volts fail signal, which is the reset output of IC32, is applied to the output enable pins of shift registers IC24, IC27, IC30 and IC36 to lower their power consumption.

4.1.12 Interprocessor Communication

The synchronous and asynchronous processors communicate with each other using the port A lines and the associated port C Buffer Full output and Strobe input lines of the RAM I/O Timers IC18 and IC6. The port A lines of IC18 and IC6 are connected together to exchange information while the Strobe and Buffer Full lines are cross coupled through inverters to exchange the handshake control signals. IC34D is used to turn off the Strobe signals to the synchronous processor in the event of failure of the AC power, since a constant low on the Strobe input would hang up the processor.

Communication between the processors occurs as follows:

The transmitting processor writes the character to be sent from port A and creates a high pulse on its Buffer Full line. This high pulse produces a low pulse on the receiving processor Strobe line that creates an interrupt from the INTR output. It also raises the Buffer Full line on the receiving processor which, in turn, is read on the Strobe input of the transmitting processor. When the receiving processor reads the character in port A, the Buffer Full line drops automatically again raising the Strobe line on the transmitting processor. This informs the transmitting processor that the character has been read and that the receiving processor is ready for another character, at which point the sequence continues.

Character interchange between the processors takes place several times per second. Each second, during the 25th frame of Time Code, the synchronous processor prompts the asynchronous for any data that it may have to transfer. At this point, the asynchronous processor may send any data such as the time, if required by the synchronous processor, or any offsets that have to be carried out during the next second or it may request the date.

When the asynchronous processor provides the time over the RS232 interface or the telephone line, it must create a carriage return that terminates at precisely the top of the second. This carriage return is used by the equipment receiving the time data to determine the start of the second. The synchronous processor cues the asynchronous processor 33 ms (one carriage return duration) before the end of each second. The asynchronous processor is then able to start the carriage return at the correct moment.

Immediately before the top of each second, the synchronous processor sends four characters to the asynchronous processor detailing its status and the time. The synchronous processor status indicates if the processor knows the time, if it has detected ringing on the telephone line, if it knows the impulse clock time and if it is correcting the impulse clocks. The state of whether the synchronous processor knows the impulse clock time or whether it is correcting the impulse clocks, is used by the asynchronous processor to determine the state of the Impulse Clock Correction Mode LED of the front panel.

4.1.13 Asynchronous Processor

The circuitry of the asynchronous processor IC5 is very similar to that of the synchronous processor. It uses the same basic circuit configuration as well as the same address decoding scheme. The two EPROMs IC7 and IC8 provide 16k of code. Input data is read by input buffers IC2 and IC3 and output data to the modem card is sent via output latch IC13.

The asynchronous processor communicates with the 5300CA Control Assembly module via data buffer IC14 and gates in IC10, IC11 and IC23. The control assembly is configured as a memory mapped device occupying 8 addresses that start at 4000 Hex. The 8 addresses are obtained from lines A0 to A2 of address demultiplexer IC12, buffered by IC10A, B and C and sent to the 5300CA module via pins A10, A11, and A12. Module enable pulses are created by ORing the processor read and write signals respectively with the 4000 Hex address select line from the address decoder IC9 in gates IC11A and C. This provides the control assembly read enable and the control assembly write enable signals which, in turn, are ANDed in IC23C to control the enable input of the bidirectional data bus buffer IC14. The control assembly read signal is also used to determine the direction of the buffer.

4.1.14 Display Control

The 8 addresses from IC10A, B and C are sent to the 5300CA module to control the selection of the six digits of either the front or rear display of the control assembly. The first six addresses correspond to the six digit drive circuits. Writing to the seventh address causes the display information to appear in the six digits of the rear display. The eighth address causes the

information to appear on the front display. These functions toggle so the information appears only on one set of digits at a time.

The A inputs of the bidirectional buffer IC14 are connected to the asynchronous processor data bus while the B inputs of IC14 are connected to the 5300CA module data bus. The direction of the data flow between input A and B of IC14 is determined by the control assembly read enable signal from pin 3 of IC11A which is applied to the direction select pin of IC14.

4.1.15 Keyboard Control

Whenever a front panel key is pressed, the 5300CA module sends a low strobe pulse to pin 15 of input buffer IC2. The control assembly read signal from IC11A enables the keyboard BCD code to lines D0 to D3 of data buffer IC14 and the shift code to line D7 of IC14. When enabled by IC23C, IC14 gates the keyboard BCD code to the asynchronous processor data bus. This will provide the processor with the code corresponding to the key that was pressed. Reading any of the eight addresses of the control assembly will reset the keyboard Strobe output.

4.1.16 Keyboard Beep

Depending on the setting of the keyboard beep enable switch S2 located at the front of the 5300ET module, a beep tone will be produced whenever a key is pressed on the keyboard. When a key closure is made, a single short beep signal is created at pin 30 of the RAM I/O Timer IC6. This beep signal is buffered by IC17A and applied to a speaker on the 5300ET module. In the case of an incorrect key closure, the short beep will be instantly followed by a longer beep of higher frequency to provide an error indication. Turning off switch S2 will silence the keyboard operation.

4.1.17 Non-Volatile EEPROM

The asynchronous processor uses the Electrically Erasable PROM IC4 for non-volatile storage of data such as the device serial number and the telephone number required for time updates. EEPROM IC4 is driven by port B, bits 2, 3, and 4, of the RAM I/O Timer IC6. Port B2 is used in bidirectional mode as the data input and output to the EEPROM. Port B3 is used as the serial clock to the EEPROM and port B4 is used as the select input to the EEPROM.

NOTE: If 5300ET modules are exchanged between units, the device serial number stored in the EEPROM IC4 will no longer match the serial number of the unit. This will lead to difficulties entering the system mode.

4.1.18 Modem Interface

Output latch IC13, parts of port B of IC6 and input buffers IC2 and IC3 are used as an interface to the 5300MB Modem Board module. IC3 latches the data from the data bus when it receives a latch pulse. The latch pulse is created in IC11B by gating the processor write line and the 6000Hex address select from IC9. The lower four bits of IC13 are the DTMF Code for tone dialing on the 5300MB module and the next most significant bit is the DTMF enable to the tone dial circuit. The remaining three bits of IC13 control the originate/ answer mode, the squelch transmitter mode and the analog loop-back mode of the 5300MB module. Port B5 of IC6 at pin 34, is used as the seize line command for the 5300MB module.

When the 5300MB module is present, pin B4 of the 5300ET module edge connector will be grounded. This is detected by pin 13 of input buffer IC3 which indicates to the asynchronous processor that the module is present. The carrier detect from the 5300MB module is sent to pin 6 of input buffer IC2 while the received data from the 5300MB module is read in pin 2 of IC2. Modem transmit data is originated from the asynchronous processor through port B0, pin 29 of the RAM I/O Timer IC6.

When enabled, switch S3 of the front of the 5300ET module allows full system mode access to any user via the telephone line. When switch S3 is turned off access to system mode is not allowed from the telephone line. Access to system mode is, however, available at all times on the RS232 input.

4.1.19 RS232 Interface

The asynchronous processor supports a complete 300 baud RS232 interface. All serial communications are done within the processor itself and no hardware UART is required. RS232 transmit data originates on port B7 pin 36 of IC6 and Clear-To-Send originates from port B6 pin 35 of the same device. The RS232 output buffer IC16 is powered by IC38 to create the required negative supply voltage for the RS232 signaling. In addition to the transmit data and Clear-To-Send handshaking which are controlled by the processor, the Data Set Ready and Data Carrier Detect lines for the RS232 interface are held asserted by IC16 at all times the power is on.

The RS232 received data is buffered to the asynchronous processor circuitry by IC17D. Received data goes into pin 8 of the input buffer IC2. The incoming Request-To-Send handshaking line is buffered by IC17C and read by pin 11 of IC2.

4.1.20 External Reference

When an external reference is applied to the CSD-5300 unit, the asynchronous processor detects the presence of the external reference via IC2, and uses this information to light the External Reference LED on the front panel. When a new time is being sent to the CSD-5300 unit and an external strobe is used to synchronize the unit to the external source, the external strobe information from the auxiliary output connector is buffered by IC15A and fed to pin 8 of the second input buffer IC3. IC3, in turn, sends this information to the asynchronous processor data bus.

4.1.21 Power Supply

The circuitry in the 5300ET module has been designed so that the synchronous processor will continue operating on battery power during a failure of the AC supply to the CSD-5300 unit. For this reason, many of the buffer circuits feeding the asynchronous processor data from the synchronous processor are of the 74HC4049 type which do not load down their inputs when the power supply to the circuit fails. This has been done to cut power drain from the synchronous processor while the asynchronous processor is not operational.

The 5300ET module receives +5 V and +13 V from the 5300PS Power Supply module and +9 V from the internal battery. In the case of a power failure, only time keeping circuitry such as the synchronous processor and related circuits is kept operational for approximately 8 hours by the internal battery.

The +9 Volts from the battery is fed to IC46, a Low Dropout voltage regulator. Its output provides a regulated +5 volt supply which is connected to the +5 V supply from the 5300PS module via diode D3. This allows the +5 V supply to take over in case regulator IC46 fails.

4.2 5300ET Electronic Timer Schematic

Chapter 5

5300 Master Oscillator Module

5.1 Circuit Description

The 5300MO Master Oscillator module provides the main time base for the CSD-5300 Clock System Driver unit. It consists of a high stability, ovenized, 15 MHz crystal oscillator that can be locked to a 5 or 10 MHz external reference. All the frequencies required by the time keeping circuitry of the CSD-5300 unit are derived from this oscillator. The 5300MO module also provides a 5 MHz output, 75 Ω, at approximately 2 Vp-p.

5.1.1 Crystal Oscillator

The crystal oscillator is a two-stage 15 MHz Butler oscillator with a third overtone crystal. A varactor diode provides the frequency adjustment capability required for either free run operation or for locking to an external reference.

The entire oscillator assembly, including the crystal and active and passive components, is housed in a temperature controlled oven assembly. Power transistor Q102 is the heating element for the oven assembly. Drive for this transistor is provided by transistor Q1 which, in turn, is driven by the Operational Amplifier IC11. The temperature sensing element is a 2.7k sensistor mounted in the oven block which also houses the crystal, the active components of the oscillator and the heater transistor. Thermo-feedback from the heater Q102 to the sensistor is used to close the feedback loop formed by IC11, Q1 and Q102. The oven assembly runs at approximately 60°C. The exact temperature is set by a SOT (select on test) resistor in series with the 3.32 kΩ resistor connected between pin 3 of IC11 and ground. The actual oven temperature is adjusted to the upper turn over point of the crystal in order to minimize frequency variation with slight changes in temperature.

5.1.2 Main Clock Reference

The output of the oscillator at the emitter of Q101B is coupled, through a tuned network, into the CMOS Hex inverter IC7F where it is squared and converted to a logic level suitable for subsequent processing.

The resulting 15 MHz logic level from the output of IC7E at pin 10 follows several different paths. First, it is fed to the two divide-by-five circuits IC5C and B where the signal is divided by 25. The resulting 600 kHz output is sent to the 5300ET module where it is used as the main clock reference frequency.

5.1.3 System Clock

The 15 MHz is also fed to IC8A and B which are configured as a divide-by-3 counter to provide outputs of 5 MHz. The 5 MHz output is fed directly to pin 6 of NOR gate IC3B and, via a delay circuit consisting of IC4A and F and

associated components, to pin 5 of IC3B. The output of IC3B is an approximately square 5 MHz wave. This signal is buffered by IC4C and D and exits the module at pin 3, where it is sent to the 5300ET module to be used as the main microprocessor clock.

5.1.4 5 MHz Reference Output Signal

The 5 MHz from IC3B is also buffered by IC10F and then fed to the remaining five sections of IC10 (A through E). The five sections of IC10 are connected in parallel to provide sufficient drive for the tune impedance matching network which consists of a 102 Ω resistor, a 2.7 μF inductor and associated components. Since this part of the circuitry does not require battery back-up in the event of a power failure, IC10 is supplied by its own 5 Volts regulator. The output of the matching network exits the module at pin M as a sinusoid of approximately 2 Vp-p, terminated into 75 Ω.

5.1.5 100 kHz/1 MHz Reference Output

The 5 MHz from IC8B is divided by 5 in IC9C. The resulting 1 MHz is fed directly to a jumper as well as converted to 100 kHz by the divide-by-5 IC9B and the divide-by-2 IC9A and then fed to the second pin of the same jumper. The jumper selects either 100 kHz or 1 MHz which is sent to pin 37 of the Auxiliary Connector for use as a reference output.

5.1.6 External Reference

The 5 MHz from pin 8 of IC8B is divided by 5 in IC9D. The resulting 1 MHz signal is fed to one of the inputs of the phase comparator formed by IC2A, IC2B, IC3C and IC3D. The other input to the phase comparator comes from a jumper that selects the frequency of the external reference.

The external reference consists of a 2 Vp-p signal of either 5 or 10 MHz. It comes from a 75 Ω loop-through on the rear panel and enters the 5300MO module at pin F. It is AC coupled, peak to peak detected by D4 and D5 and buffered by transistors Q2 and Q3 before being sent to the 5300ET module for indication of an external reference present.

If no external reference is present, the output of Q3 will be high. This is applied to pin 8 of IC3C which will set IC2A and B, forcing a low at pin 8 of IC2B and a high at pin 5 of IC2A. Thus, diodes D1 and D2 will be off and the phase comparator will be disconnected from the frequency control amplifier IC1. The output of IC1, as it appears at the control voltage test point, will be nominally 2.5 Volts. However, it can be adjusted approximately ±1 Volt by the frequency control potentiometer located at the front of the module. The output of IC1 is coupled through a 100 kΩ resistor and a 330 kΩ resistor to +5 Volts and fed to the varicap frequency control input of the oven assembly. If an

external reference signal is present, the phase comparator is activated and the output of the 15 MHz oscillator becomes phased-locked to the external reference.

5.2 Oscillator Calibration Procedure

To maintain optimum system performance, the oscillator should be recalibrated at least once a year. The calibration procedure is as follows:

CAUTION: The stability of this oscillator is superior to the majority of general purpose frequency counters available on the market. Unless an accurate, high stability, frequency reference is available, calibration should not be attempted. The module or unit should be returned to LEITCH Video for calibration purposes.

Remove the external reference, if present, and adjust the frequency control potentiometer located at the front of the module. An exactly 5 MHz output should be obtained at pin M, the reference output of the module.

The measurement should be done by means of a very high accuracy counter operating with a high stability reference or by means of an oscilloscope being triggered by 5 MHz while looking at the reference and adjusting for zero drift.

Due to the normal long term aging of the crystal, it may eventually become necessary to provide greater adjustment range. If this is the case, the control voltage test point should be adjusted to 2.5 Volts by means of the frequency potentiometer at the front of the module. Then, the small rubber plug of the frequency adjustment located at the back of the module should be removed and a non-metallic tweaker used to adjust the 2 to 8 pF trimmer capacitor of the oscillator assembly to recenter the oscillator frequency. Note that none of these adjustments should be performed unless the oscillator temperature is stabilized, that is, it has been turned on for at least 20 minutes.

5.3 5300MO Master Oscillator Schematic

Chapter 6

5300MB Modem Board

6.1 Circuit Description

The 5300MB Modem Board is a direct connect modem that is compatible with the Bell 103 modem signalling standard. The 5300MB module can dial in both pulse and DTMF and contains ring detection circuitry. Protection from high voltage transients is included as is a speaker to allow monitoring of calls.

6.1.1 Line Interface

Transformer T1 provides DC isolation from the telephone line. The Tip to Ring circuit is closed by relay K1 which is driven by transistor Q2 when the modem goes off hook. Spark Gap SG1 clamps incoming transients at about 350 volts. Varistor V1 clamps transients passed by the transformer at 10 volts to avoid damage to the circuitry.

Jumper JU1 is installed for connection to RJ12 and RJ13 type telephone jacks. The jumper allows relay K2 to close the A to A1 circuit when the modem goes off hook. The jumper is not installed when RJ11 type jacks are used.

6.1.2 Ring Detection Circuit

The 5300MB module is designed in accordance with the type B ringer standard. This standard requires detection of ringing for signals from 15.3 to 68 Hz at levels from 40 to 150 volts RMS. Ring voltage detection is accomplished by diodes D8 to D11 and optocoupler IC3. Ring frequency detection (and dial pulse discrimination) is accomplished by the microprocessor on the 5300ET module. The RC network connecting Tip and Ring to the diode bridge provides DC isolation and sets frequency response and sensitivity. The diode bridge rectifies the AC ringing signal and doubles the frequency. IC3 provides isolation and is buffered by IC8C. IC7B passes ringing signals only when the modem is on hook. The output of the ring detection circuit is a pulse train at twice the ringing frequency for incoming voltages exceeding approximately 35 volts RMS. Dial pulsing on the same line will appear on the output, but at too low a frequency to be accepted by the processor circuit.

6.1.3 Hybrid Circuit

The audio signals are coupled to and from the telephone line through Operational Amplifier IC2 which forms a hybrid circuit. The hybrid circuit provides transmit and receive gain and isolates the transmit signal from the receive circuitry.

The receive path signals from the line are fed to IC2A which provides a gain of approximately 5 for low level signals. High level signals are clipped by diodes D3 to D6 to protect the modem IC5 from transients. The receive output of the

hybrid circuit is applied to pin 16 of the modem and to the audio output driver IC1. Modem receive sensitivity is about -50dBm.

The transmit path signals from the DTMF encoder IC6 and the transmit signals from the modem IC are amplified by IC2B and fed to the transformer through a 330 Ω resistor. The resistor sets the impedance of the modem as seen from the telephone line at approximately 600 Ω. The amplified and inverted signals from the output of IC2B are fed to pin 2 of IC2A. The same signals, but without inversion, are also fed to pin 2 of IC2A by the 15 kΩ and 43 kΩ resistors. The addition of the inverted and non-inverted signals in IC2A results in attenuation of the transmitted signal as seen by the receive input of the modem IC. Hybrid balance, and therefore isolation, is dependent upon the impedance presented to the hybrid circuit by transformer T1. Since this impedance varies with the telephone line impedance, and is not truly resistive, the hybrid will not completely reject the transmitted signals. Modem transmit output is approximately -10.5 dBm into 600 Ω.

6.1.4 Modem Circuit

IC5 is a full duplex modem that includes tone filters and is compatible with the Bell 103 signalling standard.

The modem circuit has four operating modes, determined by the inputs on the ALB and SQT pins. These modes are as follows:

1. Tri-state:	When the ALB and SQT inputs are high, the modem is turned off.
2. Analog Loop Back:	When only the ALB input is high, the modem connects the modulator output to the demodulator input to allow self-test.
3. Squelch Transmitter:	When only the SQT input is high, the modulator is disabled. The demodulator remains active.
4. Operate:	When the ALB and SQT inputs are low, both the modulator and the demodulator are active.

The tone pairs used by the modem are as follows:

	Originate Mode		Answer Mode	
	Transmit	**Receive**	**Transmit**	**Receive**
Space	1070 Hz	2025 Hz	2025 Hz	1070 Hz
Mark	1270 Hz	2225 Hz	2225 Hz	1270 Hz

The mode is set by the O/A input of pin 13. When this input is high, IC5 is in originate mode.

An audio ground is provided by the resistive divider connected to pins 15, 18, and 19 of IC5.

Carrier detect timing is set to approximately 0.5 second by the 0.1µF capacitor connected to pin 4. Detection of a carrier causes the CD output line to go low, lighting the Carrier Detect LED on the module.

The modem circuit uses a 3.579545 MHz crystal to generate an accurate clock frequency. This oscillator runs constantly.

6.1.5 Dialing

DTMF

IC6 is a DTMF encoder. The tone pair to be output is selected by the binary code applied to pins 9, 10, 11, and 12. The binary code is latched in and the tone generation starts when the Tone Enable input goes high. Tone generation continues as long as Tone Enable is high. The 10 kΩ resistor and 33 pF capacitor connected to the Tone Enable input provide a delay corresponding to the data setup time required by IC6.

The Tone Output of IC6 is normally tri-state, but goes to 2.5 volts DC during tone output. Q1 is used to keep the output at approximately 2.5 volts when no tones are being created to minimize transients at the beginning and end of the tone bursts.

The Single Tone Enable input is used for diagnostic purposes. When this input is low, only one tone of the pair selected by the binary code is transmitted. If the Group Select input of pin 4 is high or floating, the high tone is transmitted (at approximately -4 dBm into 600 Ω). If the Group Select pin is low, the low tone of the pair is transmitted (at approximately -7 dBm into 600 Ω). Normally the combined DTMF tone pair output is approximately -2 dBm into 600 Ω.

IC6 uses a 3.579545 MHz crystal to generate an accurate clock frequency. This oscillator only runs when the Tone Enable input is high.

6.1.6 Pulse

Pulse dialing is accomplished by opening and closing the Tip and Ring circuit approximately 10 times per second. When the modem is connected to an RJ12 or RJ13 jack, the A and A1 circuit must remain closed for the duration of the call. For this reason, the Seize Line input signal drives K2 through IC8A, IC8B and Q3. A separate signal must be used to drive relay K1 for dial pulsing. When Seize Line is brought high, K1 will close, completing the Tip and Ring circuit. If the DTMF Enable signal is kept low and B0 of the DTMF code is brought high, K1 will open. The front panel Off Hook LED lights whenever K1 is closed.

6.1.7 Audio Output

IC1 drives a speaker to provide monitoring of calls. The receive output of the hybrid is used to drive IC1. At this output, the transmit and receive signals are at similar levels.

Diodes D1 and D2 clip transients before the signal is coupled to the volume pot on the front of the board. The speaker is mounted on the modem card. Maximum audio output is approximately 100 mW.

6.2 5300MB Modem Board Schematic

Chapter 7

5300 RI Reference Interface Module

7.1 Introduction

The 5300RI Reference Interface is a plug-in module designed to connect the CSD-5300 Clock System Driver to an external reference of accurate time using an RS232 interface. The source of time can be either another CSD-5300 unit (connected by modem over the telephone lines), or a variety of radio receivers specifically designed to monitor radio broadcasts of precise time information. These radio broadcasts from stations WWV and WWVB (United States), MSF (UK), DCF77 (W. Germany), and others, are maintained by government agencies to provide a source of accurate time information.

When the 5300RI is connected to a modem, the CSD-5300 can phone a remote CSD-5300 to obtain the time or answer a call and provide the time to other units. The 5300RI is used in the same manner as a 5300MB Modem Board. Its use is transparent and appears to both user and caller as a 5300MB.

When the 5300RI is interfaced to a WWV, a WWVB, or similar radio receiver, the CSD-5300 is able to access the external reference to obtain the time. The 5300RI can communicate with a variety of radio receivers having an RS232 interface. Since each receiver has its own protocol and format, the 5300RI has to be individually preprogrammed to meet the requirements of the receiver. Currently, the 5300RI will support the following radio receivers:

Manufacturer/Model	Station	Frequency	Site
Precision Standard Time Inc.			
OEM-10, Model 1010	WWV	2.5, 5, 10, 15, 20 MHz	Colorado, USA
	WWVH	2.5, 5, 10, 15, 20 MHz	Hawaii, USA
Kinemetrics, True Time Div.			
60-DC	WWVB	60 kHz	Colorado, USA
LF-DC	MSF	60 kHz	U.K.
	DCF77	77.5 kHz	Germany
468DC	GOES		Geostationary satellite
Radio Code Clocks, Cornwall, UK			
RCC8000 (with type II Serial Interface)	MSF	60 kHz	UK

Manufacturer/Model	Station	Frequency	Site
Precitel 5300RC			
	MSF	60 kHz	UK
	DCF	77.5 kHz	Germany
	France Inter	162 kHz	France
European Electronic Systems Essex, UK			
M201	MSF	60 kHz	UK
	DCF77	77.5 kHz	Germany
	WWVB	60 kHz	Colorado, USA
468DC	WWV	2.5, 5, 7.5, 10, 20 MHz	Colorado, USA
Trimble Navigation			
Acutime GPS Smart Rodal Antenna Models 18636-62 (with TAIP ASCII Protocol)			
5300 GPS			GPS Satellite

NOTE: Each receiver must be ordered for a specific transmitting station, and with an RS232 interface option. Please contact the respective manufacturer for details.

7.1.1 Connections

The 5300RI plugs into the slot marked 5300MB/RI of the CSD-5300 frame. If the upper left slot is marked 5300MB only, the clock radio will not support the 5300RI module. Connections with modems or radio receivers are made via the 25-pin D connector labelled RS232, and are located at the rear panel of the CSD-5300. The secondary channel is used for this connection, leaving the primary channel (pins 1 to 8) available for connecting the CSD-5300 to a

terminal or computer as indicated in the Installation Section. The secondary channel is wired as follows:

Pin	Signal	Direction
1, 7	Ground	-
16	Receive Data	in
14	Transmit Data	out
19	Request to Send	out
13	Clear to send	in
20	Data terminal ready	out
18	Data set ready	in
12	Data carrier detect	in
22	Ring detect	in
23	Signalling speed	in

Connection between the CSD-5300 and the DB25 connector of the receiver/ modem requires the following cable interface:

CSD-5300	Hayes Smartmodems, STI OEM-10, 1010 Precite/Leitch 5300RC	Kinemetrics 60DC, LFDC	EES Model 201	Radio Code Clocks	GPS-5300 Trimble Nav Acutime GPS 18636-62
Male DB25 connector	Male DB25 connector	Female DB25 connector	Female DB25 connector	DB25 connector	Female DB25 connector
1	1	1	1	1	1
7	7	7	7	7	7
16	3	2	2	2	3
14	2	3	3	3	2
19	4	4	5	4	-
13	5	5	4	5	-
20	20	20	6	20	-
18	6	6	20	6	-
12	8	8	-	8	-
22	22	22	-	-	-
23	12	12	-	-	-

7.1.2 DIP Switch Settings

Selection of the type of modem/receiver is made via the DIP switch located at the front of the 5300RI module.

Switch				Device
1	**2**	**3**	**4**	
UP	UP	UP	UP	Hayes Smartmodems; all models and compatibles
DOWN	UP	UP	UP	PSTI OEM-10, Mod 1010 receivers
UP	DOWN	UP	UP	Kinemetrics 60-DC, LF-DC, 468DC receivers
UP	UP	DOWN	UP	EES M201 receiver
DOWN	DOWN	UP	UP	Radio Code Clocks, RC8000, Precitel/Leitch 5300RC
DOWN	UP	DOWN	UP	Trimble Navigation Acutime GPS Receiver

The ON LINE LED will illuminate when the CSD-5300 is in direct control of the 5300RI module, such as when testing the module, originating or answering a telephone call, or when accessing the radio receiver. The LED will flash off an on when a connected modem signals that the telephone is ringing.

The RECEIVE DATA LED lights up coincident with serial data received by the 5300RI. This includes data from the radio receiver connected to the RS232 port or instructions from the CSD-5300 processor. The LED will not flash when the CSD-5300 unit is on-line via a modem as the received data is then relayed to the CSD-5300 processor directly.

7.2 Trimble Navigation Acutime GPS Smart Rodal Antenna

Models: P/N 18636-62 (WITH TAIP ASCII protocol) and compatibles

7.2.1 Installation

Before installing read the manual accompanying your GPS receiver and become familiar with its proper installation usage and adjustment. Note that the ACUTIME receiver rodal antenna has special needs as to its location and requires several minutes to initialize its satellite tracking system before it is able to provide an accurate time.

7.2.2 CSD-5300 Configuration

The CSD-5300 must be set to call for the time as described elsewhere in this manual. The phone number entered is of no consequence. Note that the time obtained from GPS receiver is UTC standard time (Greenwich mean time) and will be offset with respect to the local time according to your geographical location (time zone) and

daylight saving time. This offset is not handled automatically and must be adjusted via the 5300 front panel controls.

7.2.3 Internal Call Sequence

During a call the CSD-5300 commands the ACUTIME receiver to switch to 300 baud communication by transmitting an ASCII command:

>SPT0300,8,1,N<

sent at 4800 baud (8 bits 1 stop no parity) which is assumed to be the default communication setup for the ACUTIME unit. All ASCII bytes sent at 4800 baud are separated by ten 300 baud high bits (about 34 ms). Thus an ACUTIME receiver will not be adversely affected whether it is set to 300 or 4800 baud to begin with. All communication will fail if the receiver is set to any other than the two mentioned baud rates. Baud rate setup is followed by a 2 second pause. All subsequent communication happens at 300 baud. Following the baud rate setup the receiver is told to turn off its periodic reporting of position information (part of its default power-up setup) by transmitting an ASCII command:

>FPV00000000<

After a further pause of 2 seconds the CSD-5300 starts its series of queries for time by sending the ASCII command:

>QTM<

to which, it expects an ASCII reply in the form:

>RTMaabbccdddeeffgggghhijjkllllll;*zz<

where the lower case letters stand for ASCII characters (one for each) representing the variable sections of the message:

aa	hours
bb	minutes
cc	seconds
ddd	milliseconds
ee	day of the month
ff	month
gggg	year AD
hh	GPS/UTC time offset (in seconds); ignored
i	current fix source; accepted values: 0,1,2,3
j	number of usable satellites; accepted values: 03 or more
k	GPS/UTC offset valid flag; accepted values: 1 only
llllll	reserved; ignored
zz	checksum; ignored

The time information is expected to coincide with the start bit of the first reply message byte. The time will be rejected as invalid if the value of any of the fields with specified acceptable range fall outside of this range. The time will only be accepted if three successive time queries yield times which are consistent with the internal oscillator of the 5300. This is a robustness measure. In practice time jitter on time query results is typically ±10 ms.

NOTE: Following text reprinted by permission of Trimble Navigation.

7.2.4 General Description

GPS Acutime Antenna/Receiver assembly

The GPS Acutime 6 channel self contained antenna-receiver is designed as a zero maintenance unit readily able to interface with a wide variety of equipment. The maintenance objective has been achieved by mounting the antenna and receiver board sub-assembly in a sealed white polycarbonate housing. Trimble's long experience in marine GPS has shown that the antenna seal joint is the weakest link, being subject to extreme shear forces when the housing is struck by green water or ice chunks breaking loose from masts or rigging. We have thus eliminated this source of potential problems in the GPS Acutime design. The GPS Acutime unit has a digital interface; the unit requires only a DC voltage source to operate, providing position, velocity and a 1PPS output every second together with a hex output of UTC time.

Specifications

Reaction time:	2.5 - 3.5 minutes (average) 30 - 45 seconds with memory backup
Electrical I/O:	RS-232

Dynamic capability (Electrical only):

Velocity	Acceleration	Jerk
400 m/sec	4 g (39.2 m/sec^2	20 m/sec^3

NOTE: The unit will not give fully accurate 1PPS output unless it is installed in a static environment;

Temperature:	
Operating:	-40° C to +71° C
Non-operating:	-55° C to +85° C
Humidity:	100% condensing
Prime Power:	10/32 VDC - 2 watts nominal. Inline fuse (3A Quick Blow - to be supplied by customer externally)

The GPS Acutime is compatible with both 12 and 24 volt DC systems. The GPS Acutime has an over-voltage protection circuit designed to trip at voltages exceeding 36 volts. Over-voltage conditions may cause the in-line fuse to blow. The protection circuit automatically resets upon removal of the over-voltage condition, but the fuse may need to be replaced.

7.2.5 Computer Interface — RS-232

For connection to the RS232 serial ports of most computers it is possible to wire the Acutime unit through an RS422-RS232 converter. It is also possible for short runs to use a single ended RS422 wired in the following manner to a DB-25S plug.

Color	Function	DB-25S Pin
Violet	RX -	14
Brown	TX -	3
Orange	RX +	2
Yellow	TX +	16
Black	Ground	7 (also power ground)
DC Connection		
Red		Power +ve

This combination will operate both with and without the RS422-RS232 converter in most cases. The exceptions are found with computers having UARTS with marginal voltage thresholds.

Standard Cable Arrangement - RS 232

I/O Cable Color Code

Accutime Connection	Wire Color	Function
Pin 1	Orange	RXD (Receive Data)
Pin 2	Brown	RXD (DGPS corrections I/P)
Pin 3	Yellow	TXD (Transmit Data)
Pin 4	Violet	Signal Ground
Pin 5	Blue	1 PPS/Memory Backup
Pin 6	Black	Power Ground
Pin 7	Red	Power

NOTE: 1. Connector cable via standard Conxall screw fitting (Conxall P/N 6280-7SG-523) mounted in the base of the housing.

NOTE: 2. 1 PPS output is by pulldown of external voltage provided to open collector circuit through Pin 5. Pulse synchronized to the integer second on the falling edge. Leakage current of 100 micro amps nominal taken to maintain internal memory.

7.2.6 Dimensions:

Spigot Mount Antenna/Receiver:	147 mm diam. x 100 mm high (5.8" diam. x 3.9"high) 3/4" 18637-XX Series NPT female spigot on bottom surface for mounting Volume 1700 cc maximum (103 cubic inches) including dead space around mounting spigot.
Weight:	0.41 Kg (0.9 pound)

7.2.7 System Component Description

The Acutime GPS Antenna/Receiver system consists of 3 sub-assemblies, the Antenna/Receiver board, a polycarbonate housing, and a 15 meter connecting cable.

Antenna:

The antenna unit consists of a double dipole antenna element mounted together with the Receiver Board in a heavy duty polycarbonate housing complete with mounting cone (spigot mount).

Receiver Board:

The Board consists of the necessary hardware and firmware required for satellite signal processing and solution computation. The receiver has six processing channels, operating on the L1 frequency using the C/A code. Prime DC power is supplied from an external source, with isolation against major in-line interference. The power supply module can tolerate variations between 10 and 32 volts.

The GPS Acutime board receives the satellite signal through the antenna feed line connector. The complete process, from signal processing to digital output control, is performed by the components on the receiver board. The reference oscillator is a high-stability crystal oscillator operating at 16.368 Mhz. The synthesizer module generates several signals for use on the board. One output is the local oscillator for the mixer. Two other frequencies are generated for use by the custom integrated circuits (ICs) tracking hardware. An additional signal is used as the microprocessor clock. The mixer has additional circuitry for coupling in the antenna signal. the IF module processes the IF signal, amplifying it and limiting its bandwidth. The resulting signal is fed to the signal processing circuits.

The GPS tracking hardware is based on Trimble custom gate arrays. They contain satellite tracking circuitry, plus support circuitry for the microprocessor. The GPS Acutime has a single 16-bit microprocessor to perform both functions.

The channel signal processing circuits contain hardware for tracking the GPS satellite signals and for extracting the carrier code information as well as the navigation data at 50 bits per second. The signal processor controls the operation of the tracking hardware. The receiver continuously tracks the four satellites used for a solution and the remaining channels track up to 4 other satellites. The signal processor uses the measurements and data to compute the GPS-based position and velocity solution. The navigation processor also controls the selection of which satellites are tracked and manages the orbital information data and almanac for all of the satellites.

Radio Frequency Interface

GPS Acutime is designed to be functionally compatible with the L1 GPS satellite navigation signals as described in the GPS Specification SS-GPS-300B and ICD-GPS-200. GPS Acutime operates with the experimental Block I satellites as well as the operational Block II satellites or a combination thereof.

7.2.8 Mechanical Interface - Antenna Mounting

Choose a location for the Acutime antenna/receiver as close as possible to vertical, which has a relatively unobstructed view if the horizon, and which will be safe from damage during normal operation of the host vehicle. Dense wood or metal structures will shield Acutime from satellite signals. Acutime can receive satellite signals through glass, canvas and thin fiberglass. If you plan to install Acutime in a partially enclosed environment, test the ability of Acutime to receive satellite signals before committing to a permanent mount. The Acutime unit is designed, however, to withstand the full rigors of the elements and can therefore be mounted in an exposed external location. The only limitation is that the unit's extended performance at temperatures below -40 degrees (C or F) is not warranted. The unit will perform also when partially snow covered providing the snow is dry; ice accumulations will eventually shut off performance, only if the ice sheet is continuous. The shape of the unit has however, been selected partially to minimize rain, snow and ice accumulation.

The Acutime antenna/receiver is an active head antenna. For optimal performance, avoid locating Acutime within two feet (60 cm) of other antennas, near high vibration areas like engine housings, or near radar installations. If there is a limitation on available mounting locations ensure at least that Acutime is positioned outside the radar's cone of transmission. Follow the same guidelines when installing the Acutime near satellite communication equipment (e.g. Inmarsat A or C) or microwave dishes. For best results, mount the Acutime below and at least ten feet (3 meters) away from satellite communication equipment.

If the unit is being mounted permanently in a microwave installation, e.g. for timing purposes, then care should be exercised to shield the unit from random

back-scatter from microwave dishes. Difficulties will be immediately apparent if the unit cannot lock on to satellites or shows a poor ability to track. Protection is afforded by use of a ground plane, a metallic shield which is mounted below the desired minimum viewing angle of the antenna unit. In extreme cases a cone shield extending up to a 10 degree horizontal viewing angle may be tried (make allowances for snow and rain drainage!). This takes advantage of the fact that low elevation satellites have lower signal/noise ratios due to increased ionospheric absorption and therefore are less desirable for timing purposes. Such a cone shield will not work well on a moving vehicle such as a vessel because of its rolling and pitching motion.

Acutime is designed for pole mount. The threaded socket at the base of Acutime will accept both 1" - 14 thread per inch (TPI) straight thread, and a standard 3/4" - 14 TPI (NPT) pipe thread. Acutime only requires hand tightening on the pole mount. For temporary installations on a metallic surface a magnetic mount may be used (Part No. 12920-00) together with an adapter (Part No. 17030) The adapter is threaded 5/8 11 (TPI), the standard survey instrument mounting thread.

The connector cable should be firmly secured to the support using cable ties so that there is little or no mechanical strain on the 7 pin connector.

NOTE: Acutime is a valuable instrument and for permanent installations it may be prudent to drill and pin the Acutime mount to discourage theft and prevent accidental loosening. If Acutime is easily removed, store it in a secure location when not in use.

7.2.9 Electrical Interface

System Power:

The Acutime electrical interface is via pins 6 (Ground) and 7 (Positive) on the 7 pin Conxall connector; these correspond to the black and red conductors respectively of the connecting cable. The power requirement is nominally 2 watts for a supply voltage of 12 Volts DC. The maximum voltage is 32 VDC. Input circuits are provided to protect Acutime inputs and outputs from off-nominal power conditions. The input is protected against over-voltage by means of an external client supplied 3A fast blow fuse. The power supply is set to blow this 26 VDC. If Acutime encounters low voltage conditions, it degrades gracefully and returns to full operation upon the restoration of power.

Lightning surge protection is built into the Acutime; the unit is tested to 25 kV on the antenna case, as well as 25 kV applied to each pin using an industry

standard test procedure of a 150 pF capacitor discharging through a 10k ohm resistor.

7.3 Hayes Smartmodems

The Hayes Smartmodem is connected between the 5300RI and the telephone system. The modem must be configured using its internal DIP switches to communicate with the 5300RI. Functional settings rather than the actual settings of individual switches are described here, as the location and number of DIP switches may vary from unit to unit. Proper switch position should be determined for each particular unit.

Data Terminal Ready	Support RS232-C DTR lead. Do not set this signal to the fixed ON setting.
Auto Answer	OFF. Modem will not automatically answer the phone.
Data Carrier Detect	Signals the actual status of the carrier. Do not set this signal to the fixed ON position.
Command Recognition	Enabled. The 5300RI sends command codes to the modem.
Telephone Line Type	Set in accordance with the telephone system type; single or multi-line installations.
Result Codes	These settings will not affect the operation of the unit as the 5300RI will change these settings via software commands.

Once the interface between the 5300RI and the modem is established, the CSD-5300 can request or provide the time as described in the Operation section of this manual. If communication problems between the CSD-5300 and the modem are experienced, test the modem and telephone system by connecting the modem to a computer terminal and making a few calls.

7.4 Important Notes for Usage with all Radio Receivers

Since the date is not specified by transmitting stations, the 5300RI will reject date information from the radio receiver and will return a date of 000000 to the CSD-5300. this data will cause the CSD-5300 to retain its current date without change.

The CSD-5300 provides a fixed telephone loopback time to compensate for delays caused in the translation of data from the receiver into CSD-5300 format and thus, DO NOT manually enter a millisecond value for the Phone offset.

Please note that radio receivers are subject to periods of poor signal reception, and can lose lock with the transmitted signal. The 5300RI will query the receiver to determine if the unit is in lock. If the receiver's data is considered to be of poor accuracy, then the 5300RI will reject the data and indicate a failed phone call by flashing the front-panel time display. The CSD-5300 status code will indicate **P** for **failed last phone update**. As such, the CSD-5300 should be set to call the receiver at a time of the day when the quality of the reception is known to be good and the receiver to be in lock. To determine when reception is best, consult the radio receiver manual. Most receivers indicate a lock condition with the transmitted signal by lighting up a front panel LED.

7.5 Installation Procedures For The Supported Receivers:

7.5.1 Precision Standard Time Inc. Receiver

Before installing, read the manual accompanying the radio receiver and become familiar with its proper installation, usage and adjustment. The receiver must be configured by setting a number of DIP switches in the receiver. The functional settings rather than the actual switch numbers and positions are described here as the location and number of switches may vary from model to model. Proper switch position should be determined for each particular model.

The RS232 port should be configured for 300 baud, 8 data bits, no parity, and 1 stop bit. Set the receiver to return the time in the 24-hour format. The Hour Offset is set according to your local time zone. The propagation delay switches are set according to the location of the receiver with respect to the transmitting stations in Colorado and Hawaii. The Daylight Savings Time (D.S.T.) switch will determine whether or not the receiver decodes the D.S.T. bit transmitted by the source and switches the receiver to daylight savings time. This should be set in accordance with individual requirements. The date information is ignored.

The CSD-5300 may now be set to call for the time as described in the Operation section of this manual. The telephone number entered is of no consequence.

The 5300RI will query the receiver with the QA command. This consists of a 6 byte code, QA0600, that requests the time in accordance with the time zone and the D.S.T. setting of the unit. The 5300RI expects to receive a 13 byte reply in the following format:

QSmmSMHxxxxx<c/r>

where:	Q	is the quality byte, indicating the receiver lock status.
	S	is the receiver DIP switch status.
	mm	is milliseconds in binary.
	S	is seconds in binary.
	M	is minutes in binary.
	H	is the hour in binary
	x	is the date, year, and unused data.
	<c/r>	is ASCII carriage return.

The time returned is assumed to coincide with the trailing edge of the stop bit of the <c/r>.

7.5.2 Kinemetrics Radio Receivers

Before installing, read the manual accompanying the radio receiver and become familiar with its proper installation, usage and adjustment. The receiver must be configured by setting a number of DIP switches in the receiver. The functional switches rather than the actual switch number of switches may vary from model to model. Proper switch position should be determined for each particular model.

The RS232 port should be configured for 300 baud, 8 data bits, no parity, and 1 stop bit. Set the receiver to return the time in the 24-hour format. The Hour Offset is set according to your local time zone. The propagation delay switches are set according to the location of the receiver with respect to the transmitting stations. The date information is ignored.

The CSD-5300 configures the receiver through a series of control commands. It places the receiver in the T mode and configures the output data, whereby the receiver returns the time on demand in the following format:

<soh> HHMMSSmmmQ <c/r> <l/f>

where:	h	is ASCII start-of-header code, $01.
	HH	is the hour, 2 bytes, in BCD.
	MM	is minutes, 2 bytes, in BCD.
	mmm	is milliseconds, 3 bytes, in BCD.
	Q	is the ‘quality’ byte, indicating lock status.
	<c/r>	is ASCII carriage return.
	<l/f>	is ASCII line feed.

The time returned is expected to coincide with the leading edge of the start bit of the <soh> character.

The following quality characters are accepted by the 5300RI to indicate that the time is accurate: blank ($20), comma ($2C), and asterisk ($2A). Any other quality bytes, indicating a loss of signal for 90 minutes or more, will cause the data to be deemed unreliable.

7.5.3 European Electronic Systems - ESS Model M201

Before installing, read the manual accompanying your radio receiver and become familiar with its proper installation, usage, and adjustment. The receiver must be configured by setting a number of DIP switches in the receiver. As the location and number of DIP switches may vary from model to model, the functional settings rather than the actual switch numbers and positions are described here. You must determine the proper switch positions for your particular receiver.

Configure the receiver’s RS232 port for 300 baud, 8 data bits, no parity bits, and 1 stop bit. Set the receiver to return the time in the 24-hour format. The Hour Offset is set according to your local time zone. The propagation delay switches are set according to your geographic location with respect to the transmitting stations. The date information is ignored.

The CSD-5300 may now be set to call and request the time as described in the manual. The phone number entered is of no consequence.

The 5300RI requests the time information from the EES receiver by activating the EES' DSR (RS232 pin 6) and CTS (RS232 pin 5) inputs. The receiver then responds by transmitting the following data via its RS232 port:

mSMHWDNYLBF	(on older units)
mSMHWDNYLBHF	(on newer units)

where:		
	m	is the milliseconds, 1 byte in BCD; hundreds/tens
	S	is the seconds, 1 byte in BCD; tens/ones
	M	is the minutes, 1 byte in BCD; tens/ones
	H	is the hours, 1 byte in BCD; tens/ones
	W	is day of week, 1 byte in BCD; 0/ones
	D	s day of month, 1 byte in BCD; 0/ones
	N	is the month, 1 byte in BCD; 0/ones
	Y	is the year, 1 byte in BCD; tens/ones
	L	is the leap year byte; $00 = not a leap year $01 = leap year
	B	is the BST byte; $00 = not BST $01 = BST
	H	is the health byte; it is $3F if the receiver is aligned to the radio service.
	F	is the frame byte $FF, which indicates the last byte in the sequence.

The time returned is expected to coincide with the time the CTS and DSR inputs to the receiver go active. The software compensates for the time required to transmit the data to the CSD-5300. Note that the EES radio receiver can provide the time only to the nearest 10 milliseconds. The 5300RI can operate successfully with both data formats of the EES radio receiver described above.

7.5.4 Radio Code Clocks Radio Receivers -RCC8000

Before installing, read the manual accompanying the radio receiver and become familiar with its proper installation, usage and adjustment. The RCC receiver must be ordered from factory with a Type 2 Serial Interface. The receiver must also be configured by setting a number of DIP switches in the receiver.

The RS232 port of the receiver should be configured for 300 baud, 7 data bits, no parity, and 2 stop bits.

When updating the time from the radio receiver, the 5300RI requests the time from the RCC8000 by sending a Time-Request byte ‘T’. The time data is returned from the receiver in the following format:

HH:MM:SS.mmm DD/MM/YY DDD W S<c/r><l/f>

where:	HH	is the hour, 2 bytes.
	MM	is the minutes, 2 bytes.
	SS	is the seconds, 2 bytes.
	mmm	is the milliseconds, 3 bytes, in BCD.
	DD/MM/YY	is the date, 8 bytes.
	DDD	is the day of the year, 3 bytes.
	W	is the day of the week.
	S	is the status byte.
	<c/r>	is the carriage return.
	<l/f>	is the line feed.

All characters are in ASCII, and the blank spaces are sent as shown ($20 in ASCII), for a total of 31 bytes.

The actual time is expected to coincide with the leading edge of the start bit of the Time-Request byte. The 5300RI adds a time offset equal to the length of the Request byte and the 31 byte data string to maintain the accuracy of the time information. The CSD-5300 will accept the time data as correct only when the Valid Time bit of the Status Byte is high and the Reject Code bit of the Status Byte is low. This ensures that the CSD-5300 will not accept invalid time data from the receiver.

7.6 Circuit Description

The circuitry of 5300RI Reference Interface module is based on the Mitsubishi M50747 microcontroller. The microcontroller interfaces on one side with the 5300ET Electronic Timer module and, on the other side, with the interface device selected by the user, be it a modem, radio receiver or some other source of reference time.

The microcontroller U9 operates at an internal clock rate of 1 MHz. This rate is obtained by dividing down the frequency of the 4 MHz crystal X1.

The microcontroller is monitored by watchdog U8. This watchdog circuit initializes the controller during power-up by momentarily lowering its pin 6. This low pulse is fed to the microcontroller reset at pin 28 of U9. The watchdog also monitors the supply voltage and the operation of the microcontroller. If the supply voltage drifts out of tolerance, or if the microcontroller fails to strobe pin 7 of the watchdog U8 at least once a second, then the watchdog will force a reset.

User selected options are enabled by the Device Select DIP switch SW1 and read by the controller U9 at pins 33 through 40.

7.7 5300ET Interface

The interface with the 5300ET module is handled by a subprogram called the MB Interface, or Modem Board Interface, since the 5300RI module appears to the CSD-5300 unit as a 5300MB module. This simplifies the operation of the unit and preserves the existing hardware and software developed for the CSD-5300 Clock Driver.

The microcontroller monitors nine control signals from the 5300ET module. These are the four DTMF codes, DTMF Enable, ORG/ANS, SQT, ALB and Seizeline. The control signals indicate when and how the 5300ET is to place an outgoing call, the phone number, dialing delays, tone or pulse dial, self-test, etc. The 5300RI responds with three control signals, that is, the Card Present, Carrier Detect and Ring Detect. The Ring Detect alerts the 5300ET when an incoming call is detected and thus, will initiate the answering process. The Ring Detect signal at P1-5 is generated by ring counter U7. A 62 Hz logic level signal is generated at pin 3 of U7 when pin 12 of U7 is taken low by pin 42 of microcontroller U9. Pin 42 of U9 is programmed to go low coincident with a low appearing at pin 11 of U7 which can be traced back to the Ring Detect input on the RS232 port at the rear of the unit.

The serial data signals ET-TXD and ET-RXD from the 5300ET module are routed, via digital multiplexers U1 and U2 and as selected by pins 24 and 25 of the microcontroller U9, to either the microcontroller UART at pins 20 and 21 of the microcontroller U9, the rear panel RS232 port via receiver/driver U11, or they will be shorted together to constitute a digital loopback to the 5300ET module for self-testing purposes. Alternatively, the microcontroller UART serial receive/transmit signals from pins 20 and 21 of U9 can be routed, via the same multiplexers U1 and U2, to the rear panel RS232 port via receiver/driver U11.

7.8 Modem/Radio Receiver Interface

The 5300RI microcontroller interfaces with the modem or radio receiver via the secondary channel of the rear panel RS232 port. The Data Set Ready, Data Carrier Detect, Ring Detect, Speed and Clear to Send are the control inputs to the 5300RI while the Request to Send and Data Terminal Read are the control outputs. Serial data is transmitted on the TXD line and received on the RXD line. The data and control signals are driven by the RS232 interface formed by U4, U5, and U11. U11 contains a voltage doubler/inverter and powers U4 and U5 with ±8V. The output of U4 is further buffered from TTL to CMOS levels by buffer U3.

The serial data signals TXD and RXD from the RS232 port are routed by digital multiplexers U1 and U2 to either the 5300ET serial data port at pins P1-5 and P1-K or to the microcontroller UART at pins 20 and 21 of U9.

7.9 Operation

Once the desired modem or radio receiver has been connected to the rear panel RS232 port, as described in the Connections section of this document, DIP switch SW1 located at the front of the 5300RI module should be set to select the specific device.

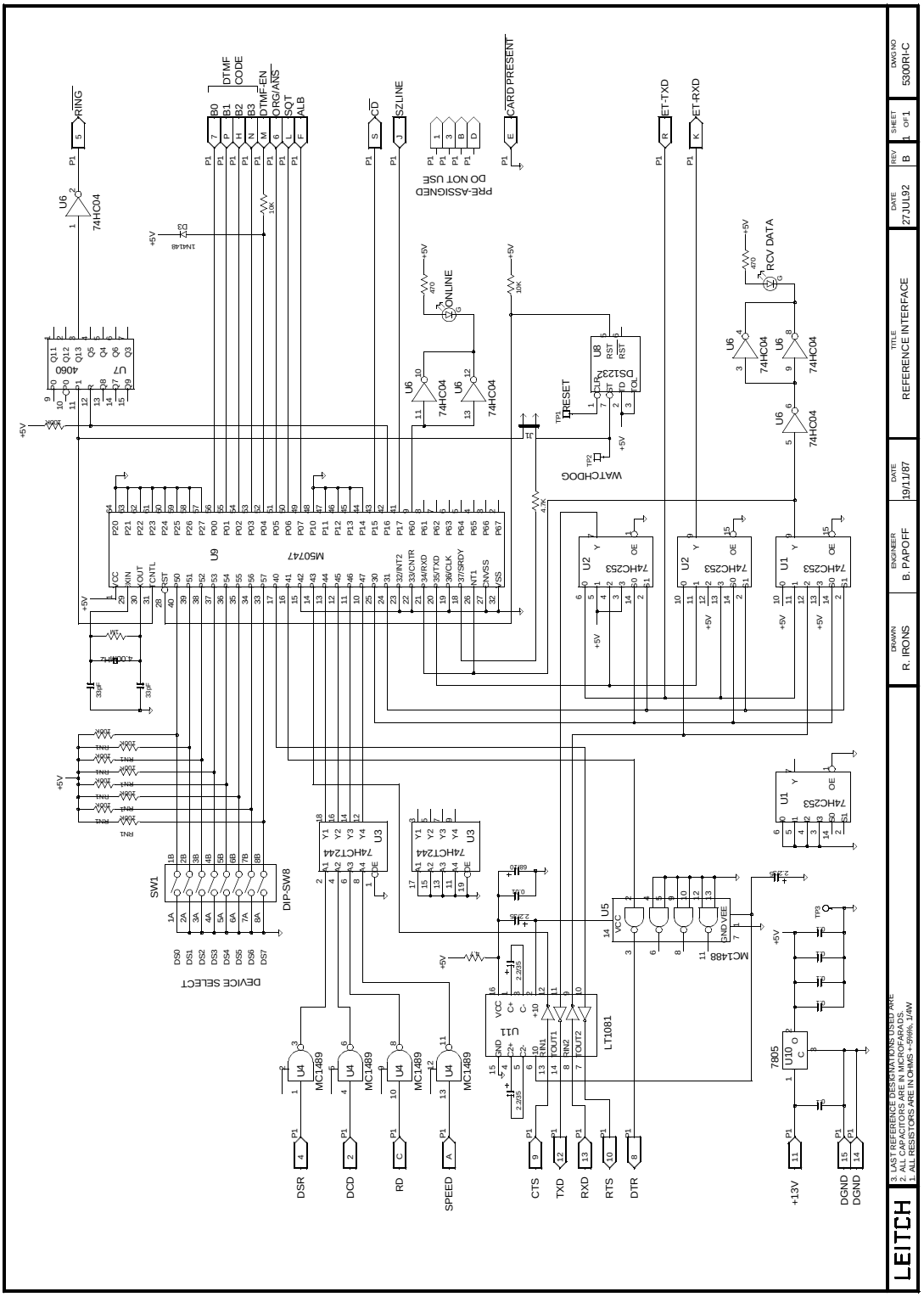
When the modem detects an incoming call, it will lower the RS232 Ring Detect Signal at pin P1-C. The microcontroller U9 senses the low signal and coincidently lowers its pin 42, enabling the ripple counter U11 and, consequently, indicating this condition to the 5300ET module. If the Telephone Answer switch on the 5300ET module is enabled, then the 5300ET will request the 5300RI module, via the control lines, to answer the phone. The 5300RI connects its UART serial data to the RS232 port via multiplexers U1 and U2, and transmits a set-up and Answer command to the modem. When the 5300RI detects a low on the RS232 Carrier Detect signal at pin P1-2, it will lower pin P1-S, the Carrier Detect signal to the 5300ET. Then the microcontroller connects the serial data lines ET-TXD and ET-RXD from the 5300ET to the serial data lines of the modem via the RS232 RXD and TXD lines. The caller then communicates directly with the 5300ET module. The microcontroller continues to monitor the Seizeline signal from the 5300ET and the Carrier Detect signal from the modem. Either one of these signals going false will cancel the call.

Similarly, the 5300ET calls out by indicating the phone number, pulse or tone dial and pauses to the 5300RI module via the control signals. The 5300RI then decodes the dialing sequence, translates the sequence to proper instructions for the modem and transmits the set-up and Dialing commands to the modem. The 5300RI also monitors the Carrier Detect signal from the modem and, when this signal goes active, it relays the signal to the 5300ET by lowering line P1-S to the 5300ET. The 5300RI then connects the serial data lines form the 5300ET to the serial data lines of the modem via the RS232 port. The 5300ET then communicates directly with the remote CSD-5300 to obtain the correct time.

If interfaced to a radio receiver, the 5300RI will not respond to a Ring Detect signal from the RS232 port. When the 5300ET initiates an outgoing call, the 5300RI detects and decodes the dialing sequence from the 5300ET. The 5300RI ignores the telephone number and connects the microcontroller UART line to the radio receiver connected to the RS232 port. The 5300RI then transmits a set-up command to the receiver to format the data and requests the time and receiver status. The 5300RI examines the status data from the receiver to confirm that the receiver is locked to the transmitting radio station. The 5300RI then locks the internal software clock to the received time. It then verifies the received data by requesting the time again and comparing the received data to the internal software clock. To be acceptable, the comparison must match on three successive attempts. The 5300RI makes a maximum of ten attempts. If the result is invalid, the 5300RI sets an internal error flag. It then connects its UART serial data lines to the serial data lines of the 5300ET module and lowers the Carrier Detect signal to the 5300ET to indicate that is ready to provide the time.

The 5300ET assumes that it is talking to another CSD-5300 and, as such, will request the status, loopback delay, time and date from the 5300RI. The 5300RI emulates another CSD-5300 and provides the data stored in its software clock to the 5300ET to compensate for any delay in calculating the time from the raw data, thus the user should not enter a millisecond phone delay to the CSD-5300 when using a radio receiver. As radio transmissions do not indicate the date, the 5300RI will provide the date as ‘00 00 00’, causing the 5300ET to keep its current date. If the 5300RI does not contain the proper time, it will send a T (Time unavailable) to the 5300ET and the CSD-5300 unit will indicate a Phone Update Failed condition by flashing the front panel display.

7.10 5300RI Schematic


RING
DTMF CODE
B0
B1
B2
B3
DTMF_EN
ORGANS
SQT
ALB
CD
SZLINE
PRE-ASSIGNED DO NOT USE
CARD PRESENT
ET-TXD
ET-RXD
RCV DATA
ONLINE
RESET
WATCHDOG
74HC04
4060
DS1233
M50747
74HC253
74HC244
MC1488
MC1489
LT1081
7805
SW1
DIP-SW8
DEVICE SELECT
DSR
DCD
RD
SPEED
CTS
TXD
RXD
RTS
DTR
+13V
DGND
DGND
LEITCH
DRAWN
R. IRONS
ENGINEER
B. PAPOFF
DATE
19/1/87
TITLE
REFERENCE INTERFACE
DATE
27JUL92
REV
B
SHEET
1 OF 1
DWG NO
5300RI-C
3. UNLESS OTHERWISE NOTED, ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS +-5%%, 1/4W
1.

Chapter 8

5300CD Clock Driver Module

8.1 Circuit Description

The 5300CD Clock Driver module converts the impulse drive provided by the 5300ET module into an alternating phase 12 volt pulse suitable to drive up to 25 impulse clocks. It also detects a successful or failed impulse drive output and reports this status to the 5300ET module. This allows the 5300ET module to ascertain the time of the impulse clocks. In addition, the 5300CD module provides short circuit and overcurrent protection as well as it ensures clean handling of the pulse drive during start-up or power failure.

8.1.1 Clock Drive

The 5 volt, negative going, 0.3 second wide pulses from the 5300ET module enter the 5300CD module at pins A and C. They are AC coupled through a 1 μF capacitor, a 3.3 MΩ pull-up resistor and a diode connected to +5 volts. This ensures that the pulses will be shut-off within approximately half a second upon failure of the 5300ET module.

The pulses are then converted into approximately 13 volt pulses by comparators IC2A and IC2C and inverted by IC1C and IC1D. The resulting pulses drive the RS flip-flop formed by gates IC1A and IC1B. The flip-flop changes state on the starting edge of each pulse. For example, when the phase 1 drive pulse goes low, the output of IC1B, at pin 4, will go high. The output of IC1B is coupled through a 4.7 kΩ resistor to the Hex FET Q2. This turns on the pull-down on the phase 2 output. Thus, each flip-flop output turns on the pull-down of the opposite phase. Consequently, one of the two Hex FETs Q1 and Q2 is always on and it corresponds to the opposite phase pulse.

Besides driving the RS flip-flop, the outputs of inverters IC1C and D generate a positive pulse on their own phase. That is, the phase 1 pulse as a negative pulse in IC1C pin 10. This is coupled through a 10 kΩ resistor to the bias driver transistor Q6 which, in turn, drives the output transistor Q4. Feedback from the collector of Q4 to the base of the bias driver transistor Q6 controls the rise time of the pulse and limits it to approximately 500 μsec. Thus, when a phase 1 drive pulse enters the module, the phase 2 output would be held low while a positive going pulse of approximately 12 volts will be generated on the phase 1 output.

The outputs of Q4 and Q5 also drive an indicator LED located at the front of the module to visually indicate that the pulse has been sent out successfully.

8.1.2 Status Report

Additional circuitry protects the output from overcurrent conditions and reports the success or the failure of the pulse to get through to the 5300ET module. For example, in the case of a short circuit on the phase 1 output, the

excessive draw of current of driver transistor Q4 will result in a voltage drop greater than half a volt on the two 3.3 Ω resistors connected in parallel to its emitter. This signal, after being level adjusted by emitter follower Q10, will turn on transistor Q11. This will force a reset condition on flip-flops IC3A and B creating a high on their Q' outputs. This high is fed to the D inputs of flip-flops IC5A and B via inverters IC4E and D.

On the other hand, the end of the incoming pulse results in a positive going edge at IC1C. This edge, after being buffered by IC4C and F, clocks the low presented by IC4E to the D input of IC5B and results in a low at its Q output. This low, representing the failure of a pulse to get through, is sent to the 5300ET module for further processing. Therefore, a failure is reported on a pulse by pulse basis.

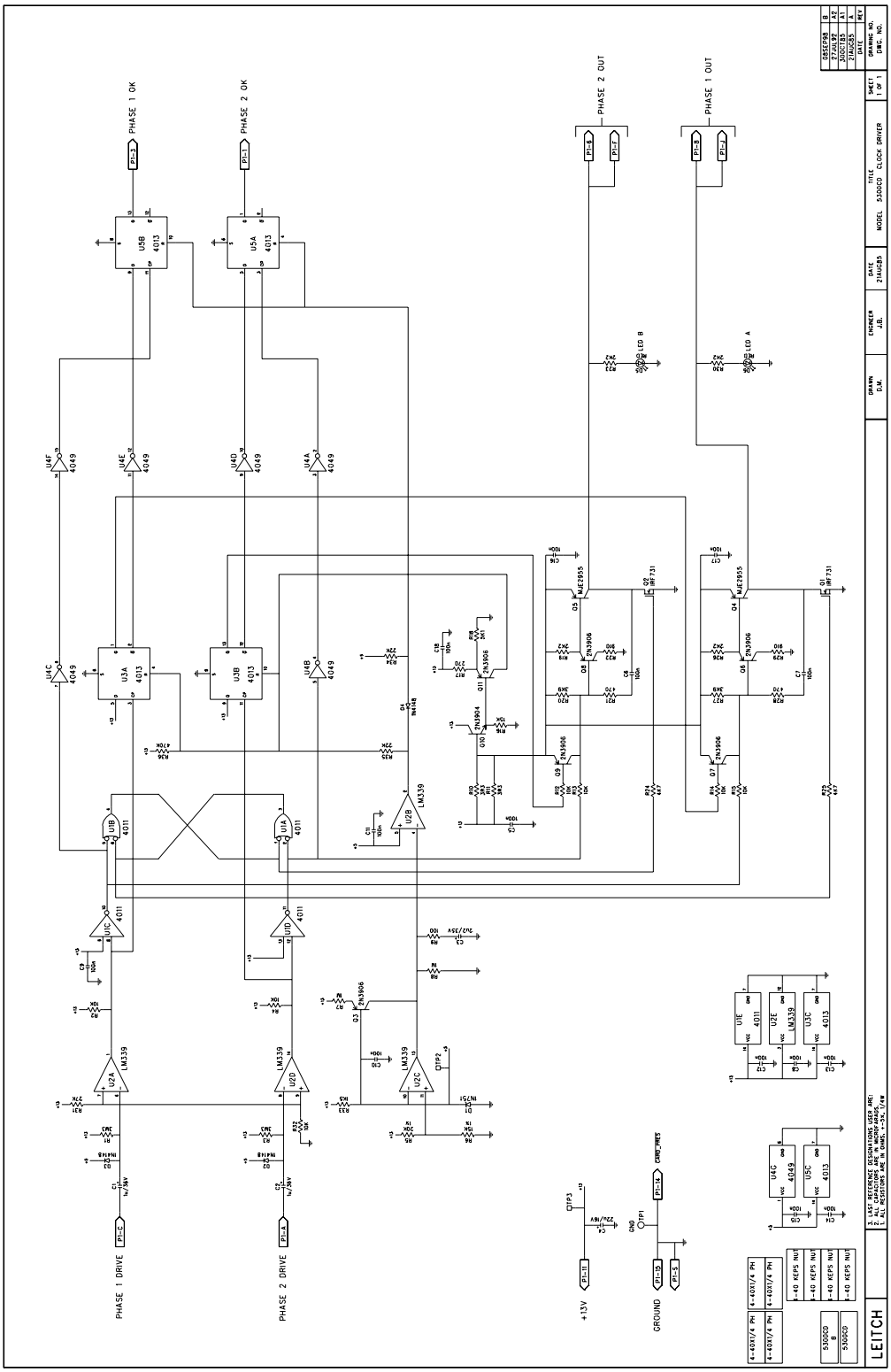
8.1.3 Overcurrent Protection

When an overcurrent condition resets IC3A and B, their Q outputs cause shut-down transistors Q7 and Q9 to turn off the phase 1 and 2 outputs. No further output drive will be attempted until the next pulse clocks IC3A and B.

8.1.4 Power Failure Detector

IC2D and associated components form a power failure detector that ensures an orderly start-up and shutdown under power failure conditions. When the incoming +13 volts is less than approximately 12 volts, the output of IC2D will be held low. This forces the output of IC2B high which, in turn, resets IC3A and B and inhibits the output drivers via shutdown transistors Q7 and Q9. It also reports that no pulse is being sent via the phase 1 OK and phase 2 OK outputs as previously described. When the +13 volts raises above 12 volts, IC2D is turned off and the 2.2 µF capacitor to ground is allowed to charge up via the current source Q3. Thus, the circuitry will be enabled approximately 1 sec. after power up.

8.2 5300CD Clock Driver Schematic


PHASE 1 OK
PHASE 2 OK
PHASE 2 OUT
PHASE 1 OUT
PHASE 1 DRIVE
PHASE 2 DRIVE
+13V
GROUND
LED B
LED A
LEITCH
MODEL 5300CD CLOCK DRIVER

Chapter 9

5300CD-24 Clock Driver Module

9.1 Circuit Description

The 5300CD-24 Clock Driver module converts the impulse drive provided by the 5300ET module into a 24 volt alternating phase pulse suitable to drive up to 25 impulse clocks. It also detects a successful or failed impulse drive output and reports this status to the 5300ET module. This allows the 5300ET module to ascertain the time of the impulse clocks. In addition the 5300CD-24 module provides overcurrent protection, as well as it ensures clean handling of the pulse drive during start-up or power failure.

9.1.1 Clock Drive

The 5 volt, negative going, 0.3 second wide pulses from the 5300ET module enter the 5300CD-24 module at pins A and C and are inverted by U8A and U8B. The circuit consisting of U7A, a 2.2 MΩ pull-up resistor, a 0.68 μF capacitor and diode D4, ensures that, in case of failure of the 5300ET module, the pulses will be disabled within approximately 0.5 seconds.

The resulting inverted pulses from U8A and B drive the RS flip-flop formed by gates U8C and U8D. The flip-flop changes state on the starting edge of each pulse. For example, when the Phase 1 Drive goes low, the output of U8C, at pin 10, will go low. The output of U8C is coupled through a 22 KΩ resistor and 10 pF capacitor to transistor Q13, the collector of which is connected to the gate input of HEX FET Q17. This turns on the pull-down on the Phase 2 output. An identical circuit turns on the Phase 1 output. Thus, the flip-flop outputs turns on the pull down of the opposite phase pulse.

The outputs of inverters U8A and U8B also generate a positive pulse on their own phase. This pulse alternatively turns on the differential amplifiers formed by Q6-Q7 and Q4-Q15 which, in turn, enable HEX FET Q10 and Q16. The approximately 37 V voltage required to turn on the HEX FET is created by the boost circuit formed by the 100Ω resistor, diode D3 and the 0.1 μF capacitor connected to the Phase 1 Output, when Q10 is off. An identical circuit is provided for the Phase 2 circuitry.

9.1.2 Status Report

Additional circuitry protects the output from overcurrent conditions and reports the success or the failure of the pulse to the 5300 ET module. For example, in the case of a short-circuit on the Phase 1 Output, the excessive current draw of transistor Q10 will result in a substantial voltage drop on the two 6.8 Ω resistors connected in parallel to its drain. This signal, after being level adjusted by emitter follower Q1, turns on transistor Q2. This forces a reset condition on flip-flops U3A and B, creating a low on their Q outputs. This low is fed to the D inputs of flip-flops U4A and B.

The end of the incoming pulse results in a negative going edge at U8A. This edge, after being inverted by U7B, clocks the low presented by U3A to the D input of U4A and results in a low at its Q output. This low, representing the failure of a pulse to get through, is sent to the 5300ET module for further processing.

9.1.3 Overcurrent Protection

When an overcurrent condition resets U3A and B, a high level from their Q outputs turns on transistors Q9 and Q12. These transistors, in turn, disable transistors Q10 and Q16 and consequently turn off the Phase 1 and 2 outputs.

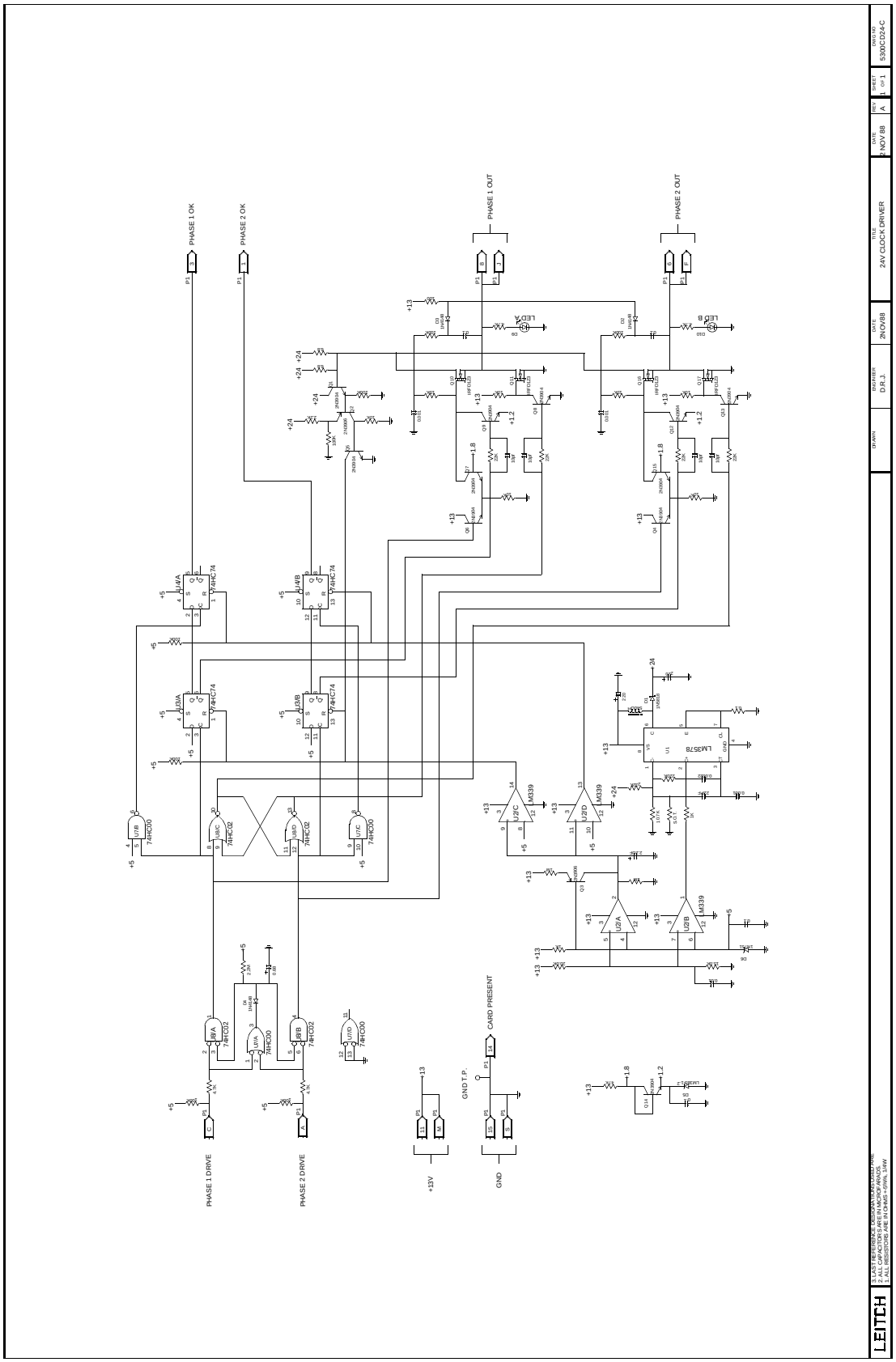
9.1.4 Power Failure Detector

U2A and associated components form a power failure detector that ensures an orderly start-up and shut-down under power failure conditions. When the incoming +13 volts is less than approximately 12 volts, the output of U2A will be held low. This forces the output of U2C and D low which, in turn, resets U3A and B and inhibits the output drivers via shut down transistors Q9 and Q12. It also reports that no pulse is being sent via the Phase 1 OK and Phase 2 OK outputs as previously described. When the +13 volts raises above 12 volts, U2A is turned off and the 2.2 µF capacitor to ground is allowed to charge up via the current source Q3. Thus, the circuitry will be enabled approximately 1 sec after power up.

9.1.5 24V Switching Regulator

U1 and associated components form a boost regulator that converts 13 V into 24 V. The regulator is turned on when the +13 V raises above 12 V. Energy is stored in the 540 µF inductor while the regulator is on, and then transferred with the input voltage to the 220 µF output capacitor for filtering, when the regulator is off. A control signal is fed back to the LM3578 comparator section for output error detection. The 0.001 µF capacitor sets the frequency of oscillator U1.

9.2 5300CD-24 Schematic


PHASE 1 OK
PHASE 2 OK
PHASE 1 OUT
PHASE 2 OUT
CARD PRESENT
GND T.P.
PHASE 1 DRIVE
PHASE 2 DRIVE
+13V
GND
LEITCH
24V CLOCK DRIVER
5300CD24-C
2NOV88
D.R.J.
A
1 OF 1

Chapter 10

5300PS Power Supply

10.1 Circuit Description

The 5300PS Power Supply module accepts an AC input between 95 and 135 Volts, 60 Hz, and an optional external battery backup voltage between 20 and 27 Volts. Either of these inputs is converted to the +5, +13, and +9 Volt power outputs required by this unit.

The circuitry of the 5300PS module consists of two power converters. The primary converter provides 27 Volts DC from the AC input and diodes it with the optional 24 Volts from the external battery. The secondary converter accepts the output of the first stage and converts it into the required power outputs.

Since these two stages are virtually identical, only the primary converter will be discussed in detail.

10.1.1 Primary Power Converter

The AC supply enters the module at pins 1/A and 3/C after being passed through the 1 Amp. magnetic circuit breaker located at the rear of the unit. It is then fed to a filter network consisting of two 0.005 μF capacitors to ground, a small toroidal filter transformer and another 0.005 μF capacitor. This filter prevents the switching noise contained in the supply from reradiating into the power line.

The AC signal is then fed to a bridge rectifier and filtered by two 33 μF capacitors and a 31 μH inductor. The resultant 160 Volts DC (for a nominal line voltage of 115) is the input to the primary power converter.

The primary power converter is a discontinuous, current mode, fly-back converter that provides an output of nominally 27 Volts. Control for this converter is provided by the controller UC3842 and timer NE555 which generates the approximately 60 kHz reference frequency for the converter.

Upon connecting AC power, the 160 Volts are applied to the primary winding of the coupled inductor and, through a 56 kΩ, 1W, bleed resistor, to pin 7 of the controller. The bleed resistor charges the 220 μF capacitor connected to pin 7 of the controller. Until the voltage of the capacitor reaches approximately 16 Volts, the internal circuitry of the controller is off, thus providing negligible current draw. Once the voltage of the capacitor reaches 16 Volts, the controller switches on, providing +5 Volts at the reference output pin 8. The +5 Volts are fed to the power supply LED to indicate when the converter is operational. It also provides the voltage required by the timer to oscillate. The 60 kHz output from pin 3 of the timer is presented to pin 4 of the controller.

When the controller switches on, its output at pin 6 provides an approximately square wave drive. This is sent to the gate of the Power Switching FET IRF731 through a 33 Ω resistor. When this signal goes high, the FET turns on and

supplies the 160 Volts across the primary of the coupled inductor. This condition is maintained until the current through the primary reaches a pre-determined value. The current is sensed by the two parallel 2.7 Ω resistors connected to the FET. The resulting low voltage signal is filtered by the 1kΩ resistor and 220 pF capacitor and presented to the current sense input of the controller at pin 3. When the current at pin 3 of the controller reaches the value determined by its voltage feed-back circuitry, the FET will go off until the beginning of the next cycle.

When the FET is off, the power stored in the coupled inductor is unloaded via two different paths. First, via the MR811 diode connected to the 220 μF capacitor and pin 7 of the controller. Second, by the secondary winding of the coupled inductor via the MR821 diode connected to the two parallel 100 μF, 35 Volt capacitors. Once the converter is on, the 56 kΩ, 1W, bleed resistor cannot provide sufficient power to drive the control circuit. Thus, the power is provided by the auxiliary winding of the coupled inductor via the MR811 diode. That is, the controller is actually bootstrapping its own power supply.

The controller output, pin 7, is applied to its feedback input, pin 2, via the 15k and 3.4k voltage divider. This voltage is compared to an internally generated 2.5 Volt reference that controls the current sensing limit at which the controller switches off on each cycle. The stability of the feedback loop is determined by the compensation components connected to pins 2 and 1 of the controller. The feedback results in approximately 13.5 Volts being maintained at pin 7 of the controller and an output voltage of approximately 27 Volts. These values are determined by the turns ratio of the auxiliary and the secondary windings of the coupled inductor.

Some energy is stored in leakage inductance and should be removed when the FET is off. This is accomplished by a dissipative clamp consisting of the high speed UES1106 diode, a 10 kΩ, 5W, resistor and a 0.22 μF capacitor connected across the coupled inductor.

The resulting 27 Volts output is connected to the 24 Volt DC supply of the external battery via a diode bridge and two 2 Amp. protection fuses. The power from the external battery enters the module at pins E and H. Since the 27 Volts are floating and a diode bridge is provided, the polarity and grounding configuration of the 24 Volts from the external battery is not significant.

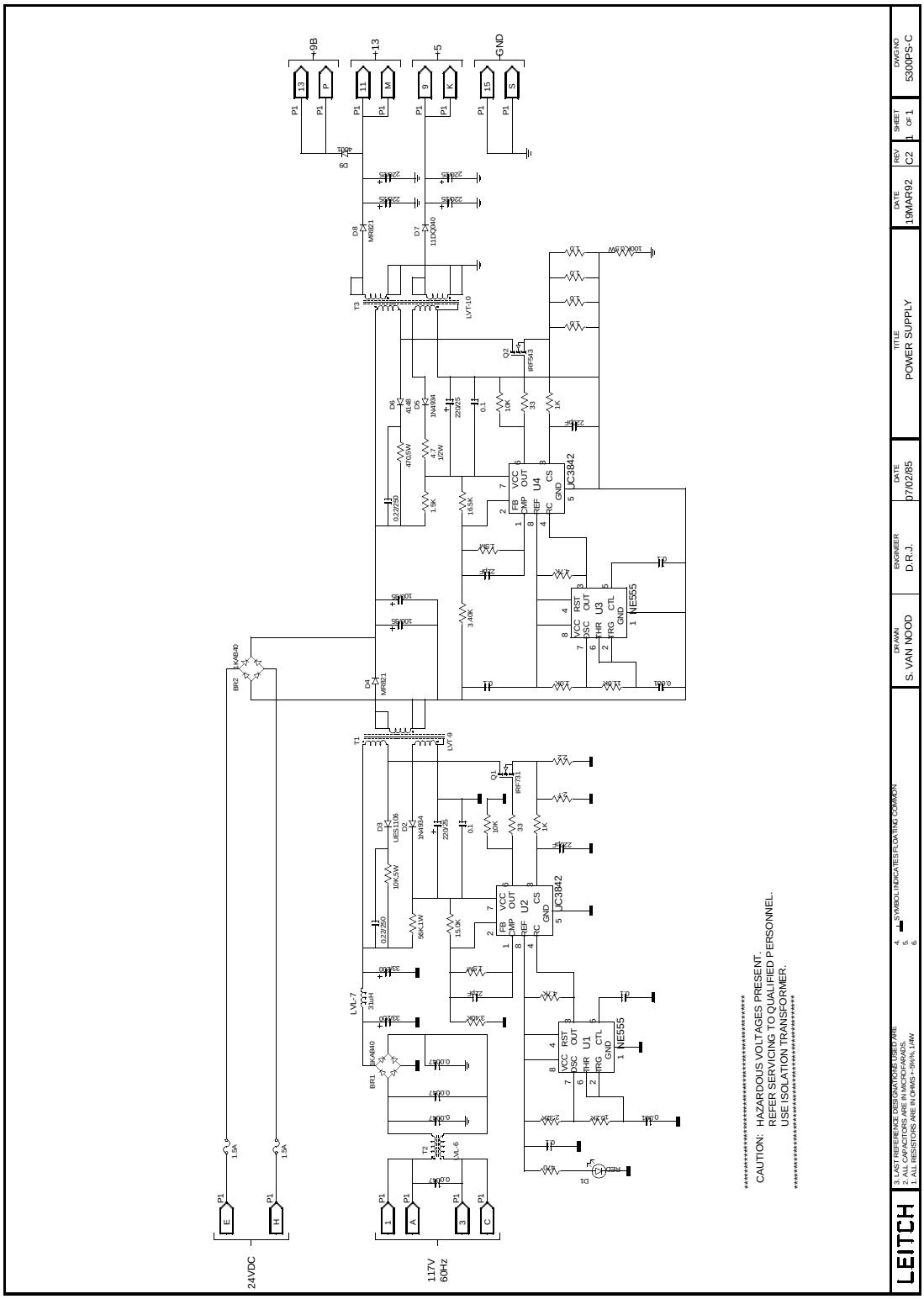
10.1.2 Secondary Power Converter

The secondary power converter accepts the 27 Volts from the primary converter or the 24 Volts from the external battery backup and converts either voltage into the power outputs required by the unit.

The power outputs are +5 Volts which exits the module at pins 9 and K, +13 Volts which exits at pins 11 and M and +9 Volts at pins 13 and P via a

1N4001 diode. The +9 Volts will be slightly over 12 Volts when either the external battery or AC is present and will drop to 9 Volts when neither AC or the external battery are present and the system reverts to its internal 9 Volt battery to maintain the primary time keeping functions of the unit.

10.2 5300PS Power Supply Schematic


+9B
+13
+5
-GND
24VDC
117V
60Hz
U1 NE555
U2 UC3842
U3 NE555
U4 UC3842
POWER SUPPLY
5300PS-C
S. VAN NOOD
D.R.J.
07/02/85
19MAR92
LEITCH
CAUTION: HAZARDOUS VOLTAGES PRESENT.
REFER SERVICING TO QUALIFIED PERSONNEL.
USE ISOLATION TRANSFORMER.