4-116. A8 PLL Multiplier Noise Generator

4-117. The A8 assembly performs several processes, all of which pertain to the oscillator signal. The main function is to accept the internal 10 MHz oscillator signal and from it produce the 500 MHz time base signal. Other signals derived from the 10 MHz input are the 100 MHz test signal, used for the Check Mode; an amplified 10 MHz signal for the rear panel; and another amplified 10 MHz signal for the plug-in accessories. Another function of the board is to phase lock the internal oscillator signal to an external reference. At appropriate times, the board also places white noise on the time base signal, thereby preventing a harmonic relationship between the time base signal and input signal.

4-118. INPUT AND MULTIPLIER CIRCUITS. The 10 MHz oscillator signal enters differential amplifier U3, which serves as an isolation amplifier. This stage prevents changing load currents from affecting the oscillator, itself. One output of the amplifier, pin 6 (TP1), is decoupled by C15 and sets the bias of Q4, 5, and 6 at 8.5 to 9 Vdc. These three transistors form one side of a differential amplifier, while the other side, Q7, accepts the output signal from U3 pin 8 (TP2).

4-119. Output Amplifiers. The output of U3 is transferred from the emitter of Q7 to the emitters of the other three transistors, which constitutes a common base configuration for these stages. There are four outputs from these stages. Q7 provides 10 MHz to the rear panel through an impedance matching network, comprised of L7, C30, and C31 (TP5). Zener diode CR14 prevents the output signal from reaching too high of a level when J2 is not loaded with 50 ohms. Another stage, Q6, sends 10 MHz to the plug-in through a similar circuit, consisting of CR15, L8, and C32 (TP6). The remaining two signals are sent to the phase detector circuit and the multiplier circuits.

4-120. Multiplier Circuits. The 10 MHz signal from Q5 feeds into a tank circuit, consisting of L9-11, C24, C26, C29, and CR12. This circuit presents two signals, 180 degrees out of phase, to the bases of Q8 and Q9. The transistors form a full-wave rectifier circuit and have the effect of doubling the frequency, while providing current gain. The resultant 20 MHz signal (TP14) is smoothed by L12 and C39, before being amplified in U5. The output signal at U5(6) feeds into the tank circuit of C42, C43, and L13. It is then fed through coupling capacitor C46 (TP15) and into the X5 multiplier of U6B, C50, C52, and L14. The multiplier output is a current square wave, which are high in odd harmonics. Tuning capacitor C52 sets the tank circuit to select the 5th harmonic of the fundamental. The resultant 100 MHz output (TP16) is amplified and filtered by U6A, C56, C57, and L15. The gain of this stage can be varied by R81 (RA). Emitter follower Q17 sends the 100 MHz signal (TP17) off the board for use as a test signal during the check mode.

4-121. The collector of Q17 passes the signal to a phase shifter circuit, comprised of L17, L18, and C68. Adjusting C68 varies the phase relationship between the 100 MHz signal and the 500 MHz signal. The 100 MHz signal can be shifted ±36°, which is 360° with respect to 500 MHz (72° x 5 = 360°). This means a full period of adjustment for synchronization between the two signals. When in the Check Mode, the adjustment eliminates the ±2 ns error incurred in a time internal measurement.

4-122. The 100 MHz signal is amplified by U7B, which uses L19 as a load. The signal passes through coupling capacitor C74, before being further amplified in U7A. The gain of U7A is controlled by R99 (RB). The last stage switches current between output transistors and produces square waves of current, which are high in odd harmonics. A quarter wave length transmission line (etched on board) and C67 (CF) tune the 500 MHz output signal (TP18). Further filtering is provided by C65, L16, C60, and C61. The final stages of amplification are provided by Q19 and Q21.

4-123. During totalize, Channel C events, or a ratio measurement, A8 turns off the 500 MHz time base signal. When the $\overline{\text{500 MHz OFF}}$ line goes low (-2V from +2V), it turns on CR19 and CR20. The diodes sink collector current from Q18 and Q20. This turns off Q19 and Q21, since they no longer receive any base current.

4-124. NOISE GENERATOR. No noise is generated when the $\overline{\text{NOISE CONTROL}}$ line is High. At this time, both Q1 and Q2 are turned on. The collector of Q2 places -15V on the cathodes of CR5 and CR6, which results in biasing U8 and U9 out of their operating range.

4-125. Once the $\overline{\text{NOISE CONTROL}}$ line goes Low, it turns on CR1 and places the emitter of Q1 at about 0.7V. This turns off Q1 and Q2 and turns on U9 and U8. The noise generated from Zener diode CR2 is amplified by U9. The noise signal couples to U8 through C12 and C11 and is amplified by U8. The cathode of peak detector CR7 sits at about 2V. The noise, therefore, must be at least -2.7V for the diode to conduct. Any noise greater than this passes through the diode and is filtered into an average dc voltage by C20 (TP12). The higher the noise, the more negative this voltage becomes. An increase of negative voltage tends to turn off Q3, thereby increasing its drain resistance. This results in more of U9's output signal being fed back to its inverting input (pin 2) and causes a corresponding drop in output voltage. The output of U8, then, is constant, due to automatic gain control.

4-126. The output noise of U8 passes through R23, C21, and R41 to the cathode of the voltage variable capacitor, CR12. This capacitor is part of a 10 MHz tank circuit, comprised of C24, C26, C29, and L9-11. As the erratic changes in noise voltage affect CR12's capacitance, the phase of the 10 MHz signal shifts rapidly. The result is a 500 MHz time base signal that is phase modulated so rapidly and erratically that it cannot be harmonically related to any input signal.

4-127. PHASE LOCK LOOP. An external signal applied tc the rear panel jack enters the board on J1. Limiting diodes CR3 and CR4 prevent excessive voltages from damaging the input circuits. The first two inverters, U2B and U2A, form a feedback trigger circuit and prevent noise from entering the circuits when no input is present. The output of U2A also feeds U2C and a delay circuit, formed by R21 and C17. The time difference between these two signals produces a positive voltage spike on U2D(15) and a negative voltage spike on U2D(9). These pulses are amplified and inverted in U1.

4-128. The phase detector circuit conducts during the time these pulses are present. During conduction, the circuit passes a small segment of the internal 10 MHz oscillator signal, which charges C33 to the value sampled. Each subsequent sample either adds to the previous charge or subtracts from it. A composite picture of many samples appears as a sine wave of the difference frequency.

4-129. When the difference frequency is too high or when the circuit is phase locked, the ac signal at TP10 is zero. At this time, Q14 and Q15 are turned on and force Q16 off. This places a High on the $\overline{\text{LAMP TEST}}$ line. The current drawn through Q14 turns on Q11, which results in shutting off Q10.

4-130. When the signal at TP10 is at a frequency that can be locked and the circuits are attempting to lock, the signal's amplitude is sufficient to drive the unlocked detector, Q12 and Q13. Diodes CR17 and CR18 pass only the positive going portions of the signal. C81 charges to a more positive level than before, which causes Q14 to turn off. Since no collector current is present, Q15 turns off, allowing Q16 to turn on and pull the $\overline{\text{LAMP TEST}}$ line Low. The gate of Q10 becomes more positive, since Q11 is also off, and allows the FET to pass the signal to the VCO on A18. Using this signal, the internal oscillator adjusts itself until it locks to the external standard.

4-131. Once the circuit locks, it opens FET Q10 and adds low pass filter R55, C45, C49, and R74 to the VCO signal line (TP11). This reduces any noise on the external standard line, connected to the back of the counter, and prevents miscounting. Rear panel switch S9 (FREQUENCY STANDARD INT-EXT) controls whether an external signal applied to the rear panel EXT FREQ STD input is used to control the counter. Q22 prevents the counter from operating off of the internal oscillator when in the EXT STD mode and the external frequency is lost or disconnected. When S9 is set to EXT, a ground is connected to Q22 emitter to enable a detector circuit composed of Q22, C84, CR21, and CR22. As long as the external frequency is present at U2D(15), Q22 is shut off. Loss of the external standard causes Q22 to conduct and initiate a front panel LAMP TEST display.

4-132. A9 Main Gate

4-133. This assembly contains 3 primary blocks: Input Selector, Main Gate, and Scaler. All input signals and reference signals (time base) are presented to the Input Selector circuits, which select only those signals needed to complete a given measurement. The Main Gate circuitry determines the precise moment these signals are passed to the scalers and, in addition, sets the