FEATURES

- 0 ~ 100MHz signal inputs
- $0.8V_{P-P}$ ~ $3.3V_{P-P}$(8~24dBm) input signal strength
- 1×10^{-12}/s Allan Deviation(ADEV) noise floor
- 50fs (5×10^{-14}s) phase difference resolution
- Matched channel delay, mismatch < $\pm2ps_{p-p}$
- Time domain frequency stability measurement for most of oscillators in the world. Reduce the use & dependence of frequency domain measurement stuffs which are expensive & huge normally (such as Phase Noise Analyzer).
- USB power & data transmit
- Only $73\times33\times120$mm(W×H×L), portable little size
- Generate ADEV/frequency difference/phase difference test reports from TimeLab software

APPLICATIONS

- **High Performance Oscillators/Clocks Stability Analyze**
  The stability analyze of high performance oscillators/clocks, such as TCXO/OCXO/Atom clocks. FSA3011 can do those frequency stability/tempco/aging measurements
- **Phase-Locked Loop Stability Analyze**
  The stability analyze of hardware PLL, quantify loop parameter
- **Disciplined Oscillators/Clocks Stability Analyze**
  - GPSDO、PPSDO output clocks frequency stability & loop stability analyze
  - 4G/5G base-station GPSDO/PPSDO performance measurement
- **Design Aid for High Performance Oscillators/Clocks**
  FSA3011 phase measurement noise floor lower than most of oscillators. In the phase of high performance oscillators/clocks design, such as oscillate circuit trouble-shot / temperature compensation / oven-tank control. Compare with traditional phase noise measurement instrument, the more design convenience can be taken by FSA3011 portable little size

BASIC BLOCK DIAGRAM

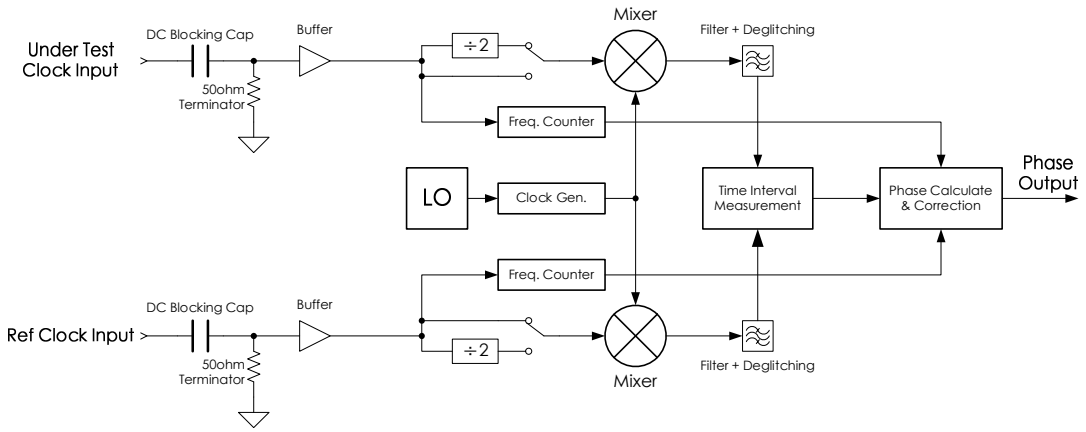
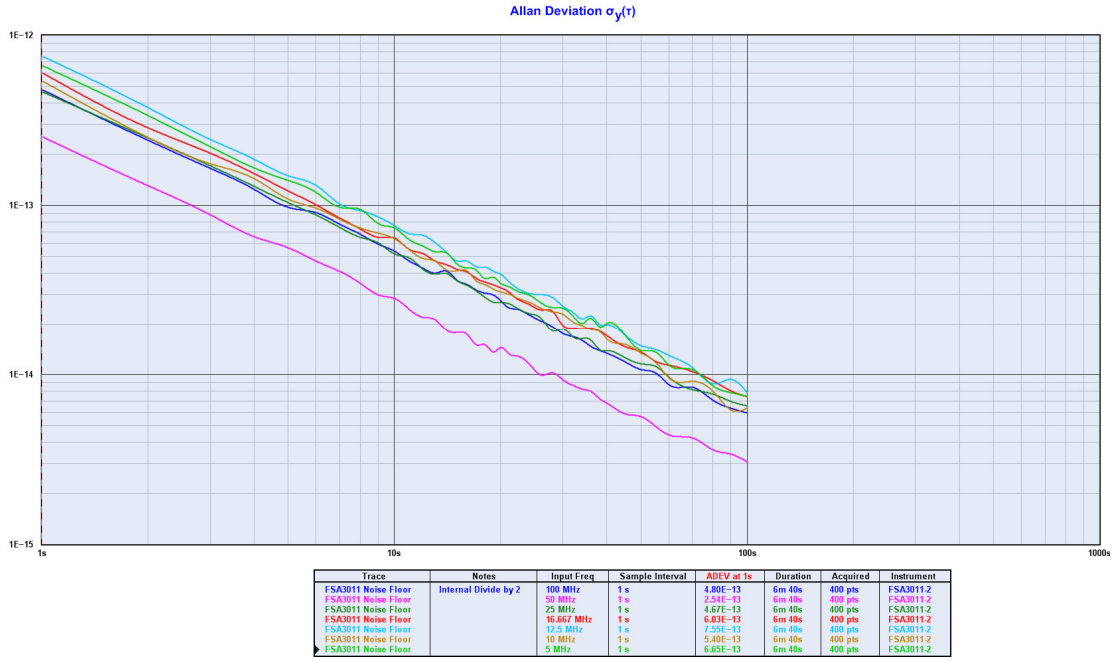


Figure 1. FSA3011Basic Block Diagram

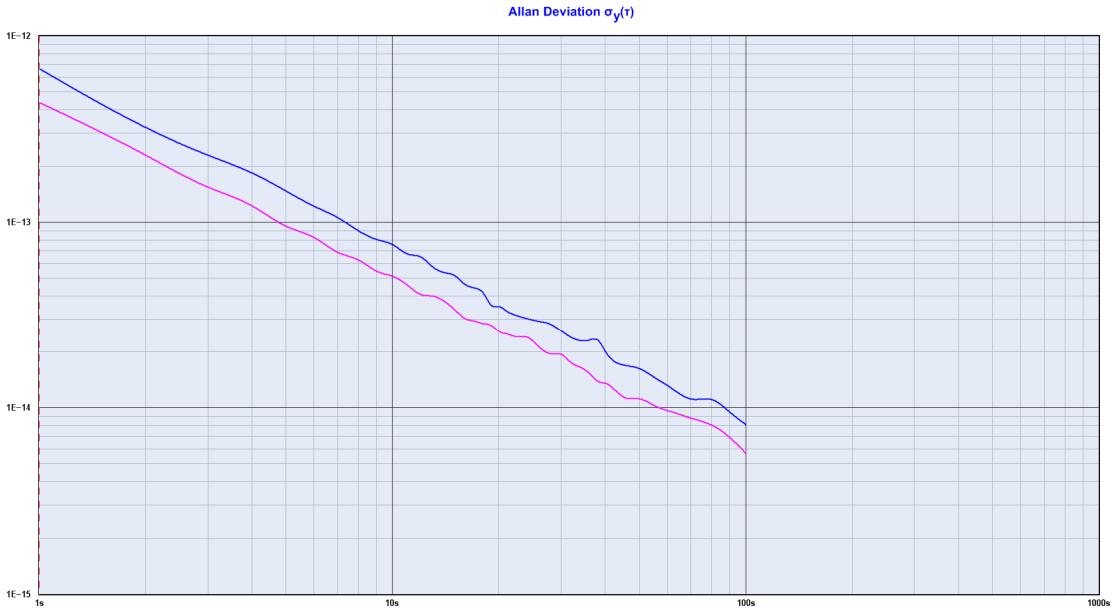
©TURN Dynamic Systems, 2018

TYPICAL PERFORMANCE CHARACTERISTICS*



Trace	Notes	Input Freq	Sample Interval	ADEV at 1s	Duration	Acquired	Instrument
FSA3011 Noise Floor	Internal Divide by 2	100 MHz	1 s	4.80E−13	6m 40s	400 pts	FSA3011-2
FSA3011 Noise Floor		50 MHz	1 s	2.54E−13	6m 40s	400 pts	FSA3011-2
FSA3011 Noise Floor		25 MHz	1 s	4.67E−13	6m 40s	400 pts	FSA3011-2
FSA3011 Noise Floor		16.667 MHz	1 s	6.03E−13	6m 40s	400 pts	FSA3011-2
FSA3011 Noise Floor		12.5 MHz	1 s	7.55E−13	6m 40s	400 pts	FSA3011-2
FSA3011 Noise Floor		10 MHz	1 s	5.40E−13	6m 40s	400 pts	FSA3011-2
FSA3011 Noise Floor		5 MHz	1 s	6.65E−13	6m 40s	400 pts	FSA3011-2

Figure 2. ADEV Noise Floor *vs* Input Frequency(3.3V_{CMOS} Input)



Trace	Notes	Input Freq	Sample Interval	ADEV at 1s	Duration	Acquired	Instrument
FSA3011 Noise Floor	SineWave(2Vp-p)	10 MHz	1 s	6.67E−13	6m 40s	400 pts	FSA3011-2
FSA3011 Noise Floor	CMOS(3.3V)	10 MHz	1 s	4.40E−13	6m 40s	400 pts	FSA3011-2

Figure 3. ADEV Noise Floor *vs* Input Signal Type

(Blue: 2$V_{p\text{-}p}$ Sine, 6.67×10^{-13}/s; Purple: 3.3V_{CMOS}, 4.40×10^{-13}/s)

*All test diagram in this document are generated by Miles Design LLC's TimeLab software.

©TURN Dynamic Systems, 2018

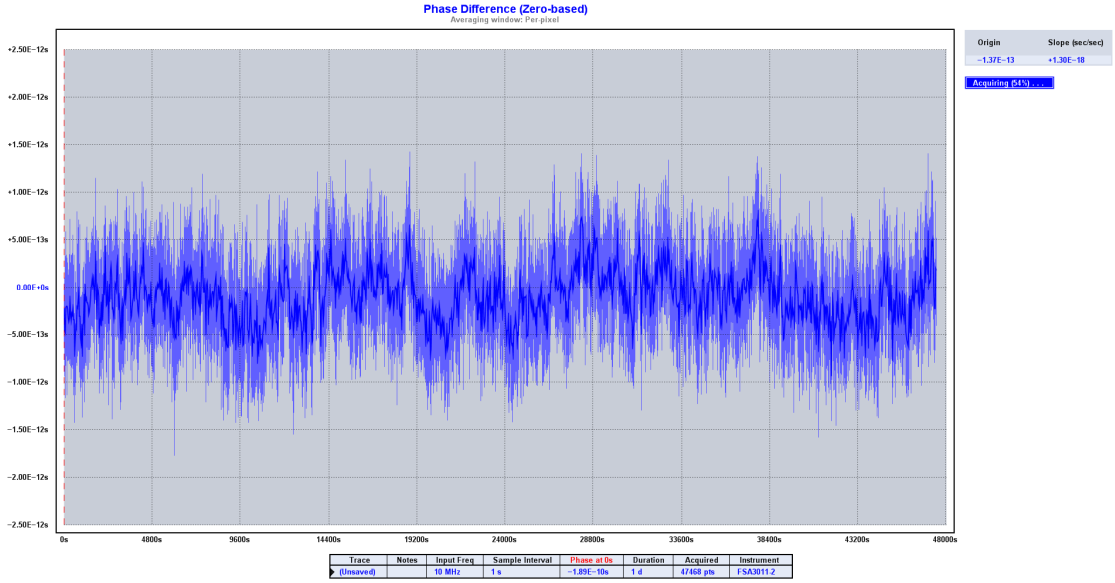


Figure 4. Phase Measurement Noise

(10MHz/Com-Source/3.3V_{CMOS} Input, No Average Applied)

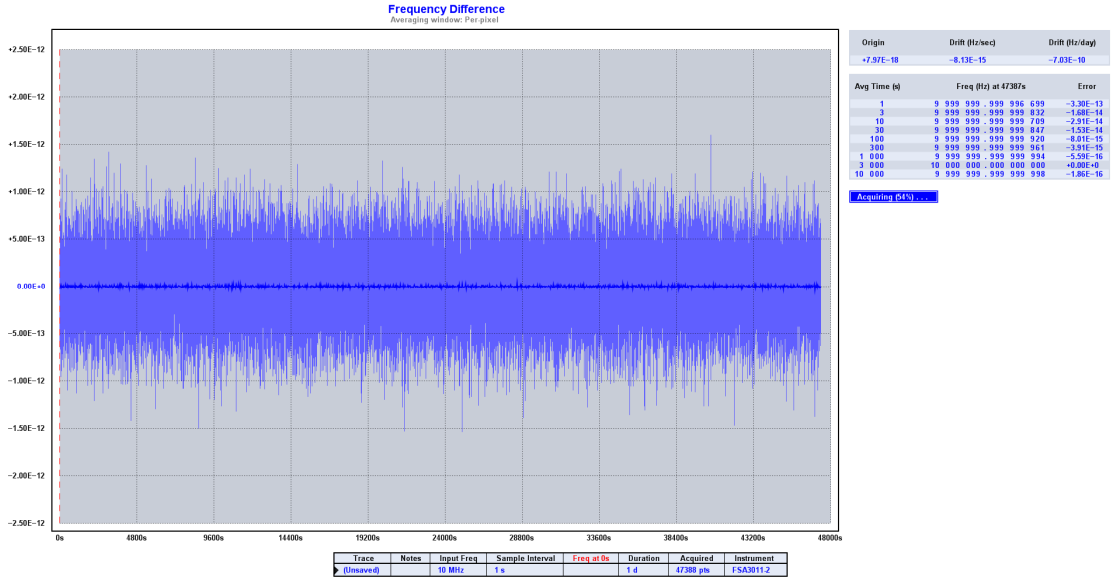


Figure 5. Frequency Measurement Noise

(10MHz/Com-Source/3.3V_{CMOS} Input, No Average Applied)

©TURN Dynamic Systems, 2018

SPECIFICATIONS

TECHNICAL SPECIFICATIONS

Parameter		Specification	Note
Ports	DUT	SMA /1-100MHz/0.8-3.3V_{P-P}/8-24dBm	50Ω Terminated
	REF	SMA /1-100MHz/0.8-3.3V_{P-P}/8-24dBm	50Ω Terminated
	USB	MicroUSB Socket/5V/500mA	USB1.1/2.0
ADEV Noise Floor	All Frequency	$< 1\times10^{-12}$/s(⩾5MHz)	3.3V_{CMOS} Input
	100MHz	$< 6\times10^{-13}$/s (typ.)	
	50 MHz	$< 3\times10^{-13}$/s (typ.)	
	25 MHz	$< 6\times10^{-13}$/s (typ.)	
	16.667 MHz	$< 7\times10^{-13}$/s (typ.)	
	12.5 MHz	$< 8\times10^{-13}$/s (typ.)	
	10MHz	$< 6\times10^{-13}$/s (typ.)	
	5MHz	$< 7\times10^{-13}$/s (typ.)	
Frequency Can be Tested		100MHz(Internal÷2); 50MHz/N (N = 1 ~ 50)	50MHz LO
Phase Measurement Noise	No Average	< 2ps(±2×10^{-12}s), Peak to Peak	10MHz 3.3V_{CMOS} Input
	10s Average	<±1ps(±1×10^{-12}s), Peak to Peak	
Frequency Measurement Noise	No Average	<±2×10^{-12}Hz, Peak to Peak	10MHz 3.3V_{CMOS} Input
	10s Average	<±2×10^{-13}Hz, Peak to Peak	
Channels Mismatch *vs* Temperature		< ±1ps/℃	

Table 1. Technical Specifications

GENERAL SPECIFICATIONS

Parameter	Specifications	Note
Power Input	5V/500mA(USB Bus-Power)	After USB Device Enumerated Success
Power Consumption	Max. 1W(5V/200mA)	
Operating Temperature	0℃-50℃	
Operating Humidity	20%-90% RH, Non-condensing	
Storage Temp./Hum.	-10℃-75℃/10%-95% RH	
Outline Size	73×33×120mm(W×H×L)	

Table 2. General Specifications

©TURN Dynamic Systems, 2018

PANEL INFORMATION

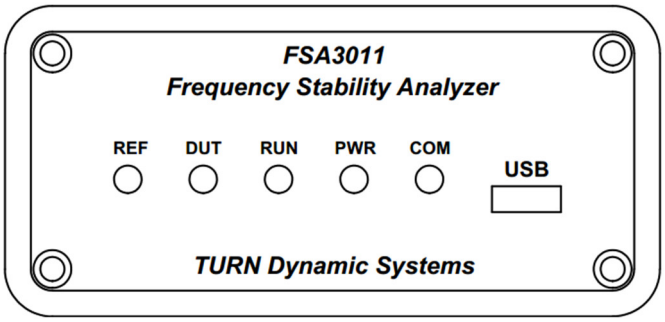


Figure 6. Front Panel

No.	Mark	Function	Note
1	REF	Indicate if Have an Active Input on REF Port	Have/Flicker Otherwise Black
2	DUT	Indicate if Have an Active Input on DUT Port	Have/Flicker Otherwise Black
3	RUN	Indicate if the Instrument is Running	Running/Fast-Flicker Otherwise Black
4	PWR	Power Up Indicator	Powered/Light Otherwise Black
5	COM	Active Data Transmit Indicator	Active Transmit/Flicker Otherwise Black
6	USB	Power Deliver & Data Transmit	Micro-USB Port

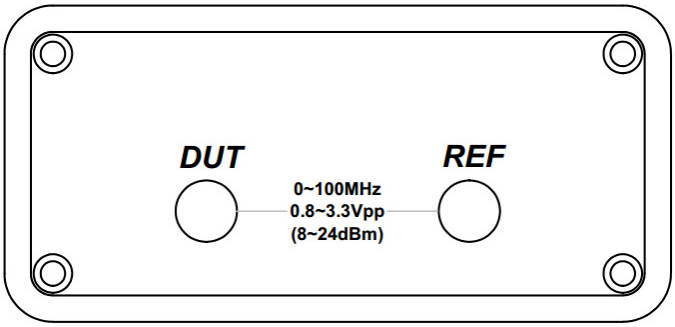


Figure 7. Rear Panel

No.	Mark	Function	Note
1	REF	Reference Clock Input	0-100MHz 0.8-3.3V_{P-P} (8-24dBm@50Ω)
2	DUT	Under Test Clock Input	0-100MHz 0.8-3.3V_{P-P} (8-24dBm@50Ω)

©TURN Dynamic Systems, 2018

TEST TOPOLOGY

NOISE FLOOR MEASUREMENT

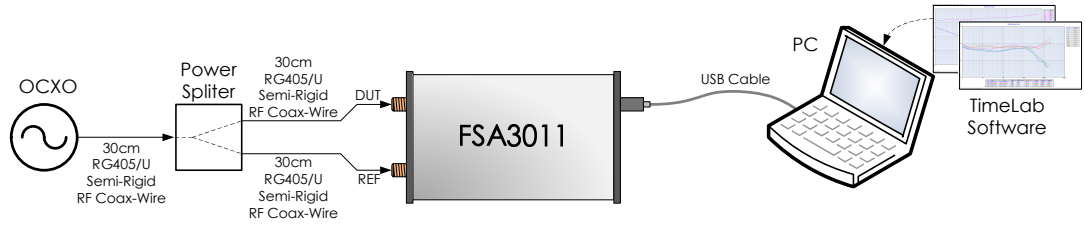


Figure 8. Signal Connections for Noise Floor Measurement (Com-Source)

The noise floor measurement of FSA3011 use the common-source method, that means DUT & Ref input signal come from the same clock source, the signal path & noise picking of two channels be considered precisely the same. So the phase fluctuation under this condition is the noise of instrument itself – that is the noise floor.

***Note 1**. Keep the same length of those two coax-cable behind power-spliter, and as short as possible.*

***Note 2**. 1 ps corresponds to a distance of 0.3mm in air(be shorter in coax-cable actually), a phase difference of 0.1ps(1x10^{-13}s) only 0.03mm(30μm). This obviously means that all signal connections must be very rigid, and the mechanical vibration/shock and strong air flow must be void on the test-bench.*

NORMAL MEASUREMENT

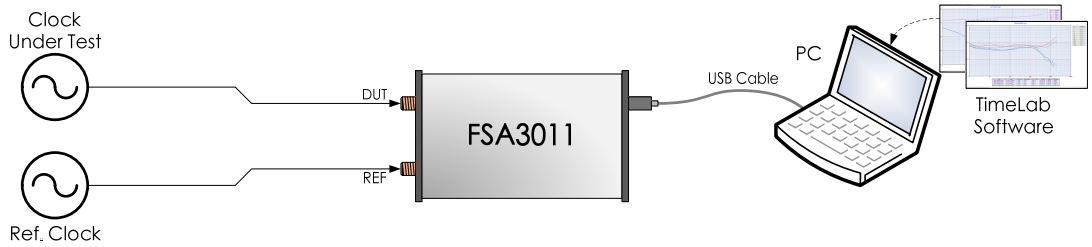


Figure 9. Signal Connections for Normal Measurement

On normal measurement. Put the high stability referenced clock source on REF input, the clock source under test on DUT input. When the test is started, FSA3011 will measure the phase difference of those two clocks precisely, and send the phase data to PC via USB, then the test reports of xDEV / phase difference / frequency difference can be generated by TimeLab Software.

***Note 1**. For high stability oscillators/clocks measurement (ADEV<10^{-11}/s), to get a higher accuracy & confidence of test result, the frequency offset between DUT & REF must smaller than 1x10^{-9}Hz.*

***Note 2**. The higher stability clock should be connected to REF input. FSA3011 correction the test data & phase difference to REF clock real-time, this makes the test result more precise and stable.*

©TURN Dynamic Systems, 2018